J18LV AC correlation of spice model to silicon

TSMC CMOS process 1.5/3.3V, 0.18um, 1P5M

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- ***Summary***

Measurements of Catwoman testchip Ring Oscillator delay are compared to simulations using TSMC supplied typical spice model 'c018njlv.l' as was DC correlated to silicon in a previous document.

Results from simulating Ring Oscillator circuits including annotated netlists provided from two tools -- Arcadia and Xcalibre -- are compared.

TSMC has apparently provided a model which attempts to be accurate *ignoring* metals interconnect parasitics. When using tools which add in estimates for metals interconnect parasitics, simulated delays increased too much. In a communication with Joanne Wu, Vicent Liu of TSMC agrees with this analysis and says that TSMC will adjust future models to more accurately include effects of extracted metal parasitics.

- ***Our Results***

The table below presents our delay measurements and simulations in a very compact form:

J18LV Catwoman Testchip Measured versus Simulated delays:

		Meas Gate Delay	Simulated, transistors only Arcadia: Delay	Error	Xcalibre: Delay	Error	Simulated with extracted parasitics Arcadia: Delay	Error	Xcalibre: Delay	Error
	site	(ps)	(ps)	(%)	(ps)	(%)	(ps)	(%)	(ps)	(%)
RO_1										
(7.5u/18u inv,	33	55.9	55.5	**-0.7**	55.0	**-1.6**	59.0	**5.5**	63.0	**12.7**
51 stages,	30	55.0	55.5	**0.9**	55.0	**0.0**	59.0	**7.3**	63.0	**14.5**
FO2.x)	28	55.2	55.5	**0.5**	55.0	**-0.4**	59.0	**6.9**	63.0	**14.1**
	29	55.5	55.5	**0.0**	55.0	**-0.9**	59.0	**6.3**	63.0	**13.5**
avg		55.4	55.5	***0.2***	55.0	***-0.7***	59.0	***6.5***	63.0	***13.7***
RO_3										
(1.4u/2.1u,	33	27.2	25.7	**-5.5**	25.1	**-7.7**	30.6	**12.5**	30.9	**13.6**
51 stages,	30	26.7	25.7	**-3.7**	25.1	**-6.0**	30.6	**14.6**	30.9	**15.7**
FO1)	28	26.3	25.7	**-2.3**	25.1	**-4.6**	30.6	**16.3**	30.9	**17.5**
	29	26.2	25.7	**-1.9**	25.1	**-4.2**	30.6	**16.8**	30.9	**17.9**
avg		26.6	25.7	***-3.4***	25.1	***-5.6***	30.6	***15.1***	30.9	***16.2***
TSMC Inv Ring										
(4u/10u,	4c	25.0	25.5	**2.0**	25.2	**0.8**	27.6	**10.4**	28.8	**15.2**
101 stages, FO1)										
overall average				***-1.2***		***-2.7***		***10.7***		***15.0***

- ***Discussion***

In the table above we show measured and simulated ring oscillator delay-per-gate information for 3 different design circuits. The 2 designed structures had data taken at 4 testchip sites, the third TSMC designed structure at only one site.

Measurements are from our first TSMC J18LV 'shuttle' lot D80123.03. Die sites 28, 29, 30,.. 33 represent separated 'sawn' die from wafer #1 of this lot. Sawn die were remounted to scrap silicon wafers using polyimide tape for ease of testing.

For each of the circuits simulated, annotated netlists were extracted from their layouts using both Synopsis Arcadia v5.3 and Mentor Xcalibre v8.7_15.5. Joanne Wu performed these extractions which resulted in spice decks with interconnect metal parasitics included. She created three more spice decks from these by manually editing out the parasitic capacitances from each deck. Avant! HSPICE 98.2 simulator was then run on all 6 decks. Spice simulations were run using J18LV, cirrus qualified typical spice model 'c018njlv.l' (TSMC v1.0' rev 0.5).

We see from the table that the model in conjunction with either tool Arcadia or Xcalibre give delays nearly equal to measured when interconnect parasitics are *not* accounted for. In the 'transistors only' columns Arcadia shows an error of –1.2% while Xcalibre shows –2.7% simulation error overall. Recall that a negative error means that simulation is faster than measured.

Simulation for the 'transistors only' case should be faster than measured so that when the slowing effects of interconnect parasitics are included the final simulation matches measured delays. When parasitics are included we see that in the Arcadia case the simulation is 5 to 16% slower and in the Xcalibre case is 13 to 18% slower than measured.

The attached graphs present a different look at simulated ring oscillator delay. These graphs will become a more valuable tool for future AC model correlations to silicon when models adjusted for interconnect parasitics are available from the foundry. For two of the designed ring oscillators RO_1 and RO_3 included in this report we plot delay per gate versus inverter stage inverse effective Idsat. Each of the 3 'diamond plots' on either graph show the 5 simulated corners of the model: typical(center symbol), fast n & p, slow n & p, fast n & slow p, and slow n & fast p. These graphs are based upon the equation 'delay per gate $\propto$ CV/Idsat'.

At this time we can use these graphs to point out the difference between using Arcadia and Xcalibre to extract interconnect parasitics. The company is switching from Arcadia to Xcalibre because Xcalibre is easier to use. There are calibration differences between the two tools which we need to understand. Note in the bottom graph for RO_1, Arcadia and Xcalibre results for the transistors (FETs) plus extracted metals parasitics case, nearly agree with each other. These simulations are done on a small, simple ring oscillator and where net extracted metals parasitic capacitances are small. As seen in the top graph for RO_3 the two tools predict very different results as observed by the vertical shift between diamonds. RO_3 is a more complex and larger design and parasitic metal capacitances are larger.

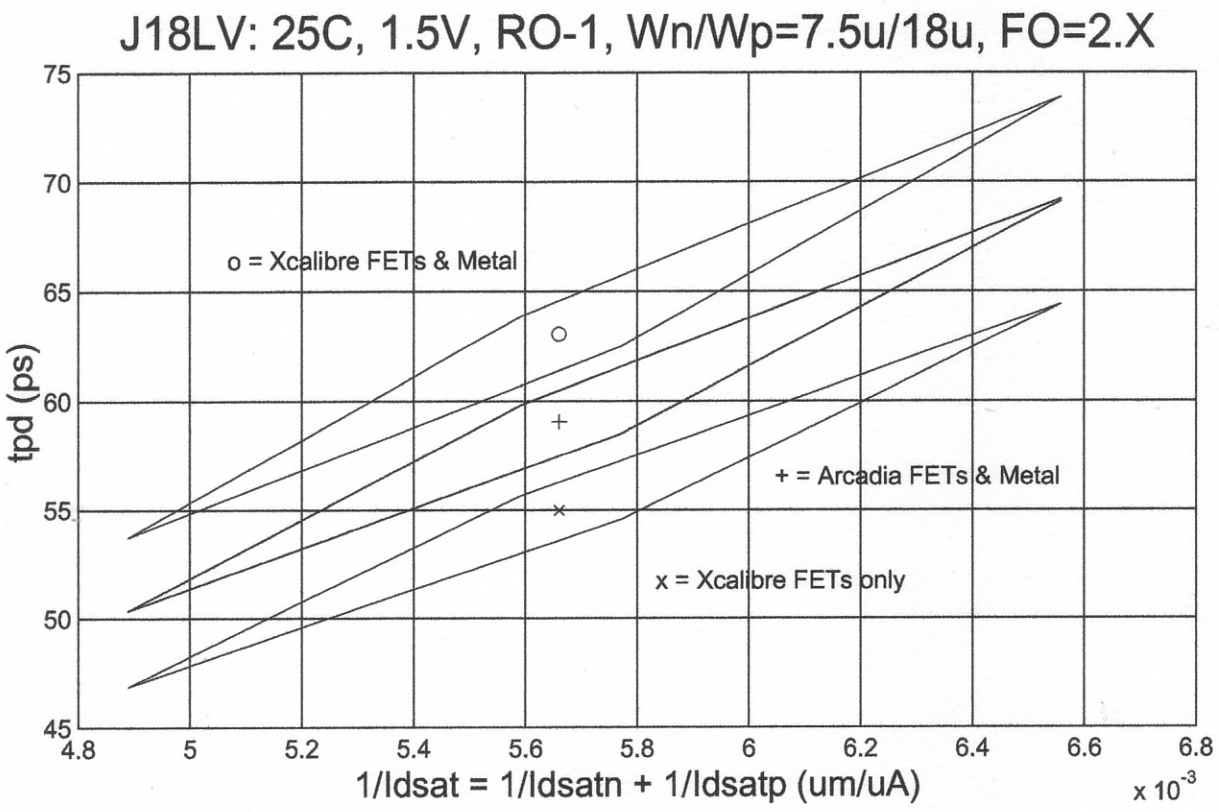
Data such as this has been shared and discussed with Mentor Xcalibre development people so that we may better use their tool.

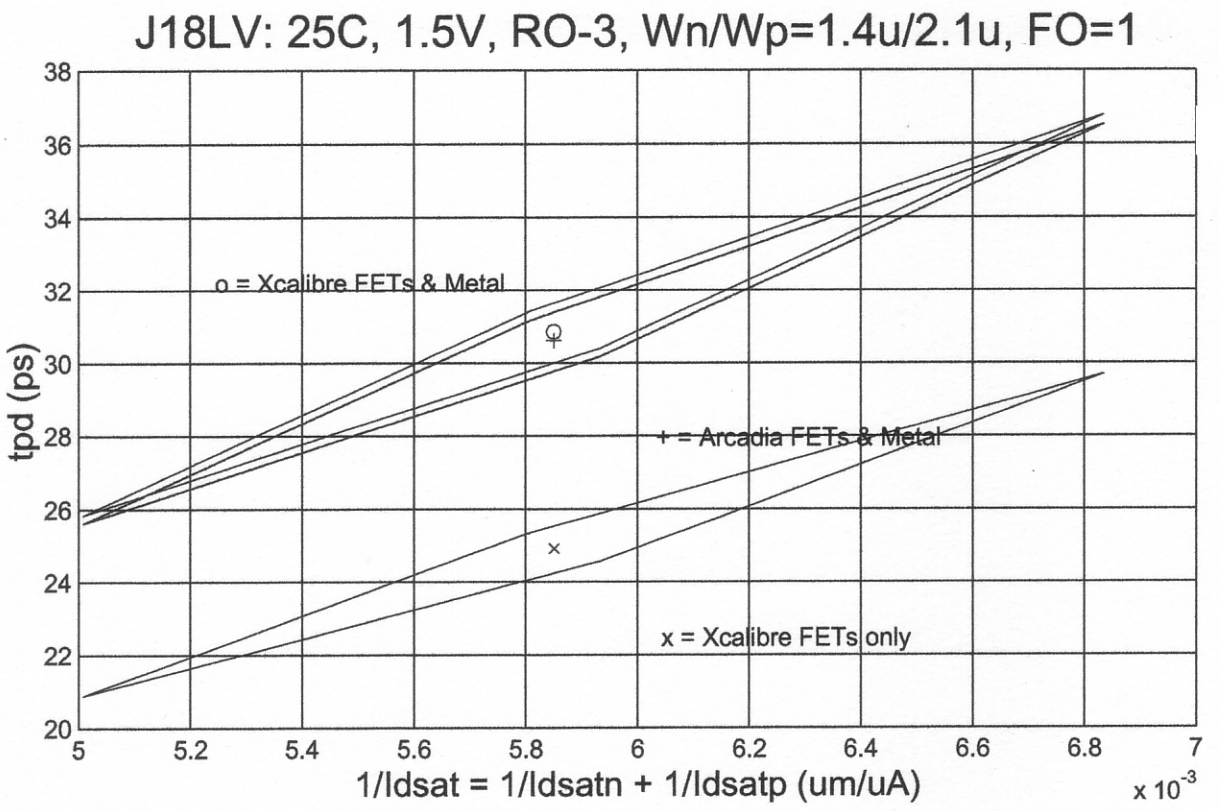
- ***Conclusions***

This report concludes that the TSMC J18LV model needs significant adjustments to handle AC (speed) simulations correctly. Capacitive and other parameters in the transistor model are too conservative and make the model slower than measurements lead us to believe.

If we more properly try to account for interconnect parasitics in our circuits this problem with the model becomes even more apparent.

Communications with TSMC show they have become aware of the problem and are taking steps to model while accounting for interconnect parasitics.


J18LV: 25C, 1.5V, RO-1, Wn/Wp=7.5u/18u, FO=2.X
tpd (ps)
75
70
65
60
55
50
45
o = Xcalibre FETs & Metal
+ = Arcadia FETs & Metal
x = Xcalibre FETs only
4.8
5
5.2
5.4
5.6
5.8
6
6.2
6.4
6.6
6.8
1/Idsat = 1/Idsatn + 1/Idsatp (um/uA)
x 10-3


J18LV: 25C, 1.5V, RO-3, Wn/Wp=1.4u/2.1u, FO=1
tpd (ps)
38
36
34
32
30
28
26
24
22
20
o = Xcalibre FETs & Metal
+ = Arcadia FETs & Metal
x = Xcalibre FETs only
5
5.2
5.4
5.6
5.8
6
6.2
6.4
6.6
6.8
7
1/Idsat = 1/Idsatn + 1/Idsatp (um/uA)
x 10-3