

# A2 Transistor Characterization Report (T1 Qual Lot)

## Device Performance Analysis

Lot No. CYS18T02

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- **Overview**

This report is based on the electrical characterization data for the A2 process from a Micrus T1 qual lot. The report provides information relating to the electrical performance of transistors. A total of 3 wafers were measured on the Micrus Lot# CYS18T02 (Wafers: S6LPGUT, SWLPK2T, SNLPKAT). Nine sites were measured on each wafer (1 site at the center, 4 sites about 3cm from the edge & 4 sites about 6cm from the edge). The testing was done using the automatic prober in the Device Lab. The data from all the sites & wafers is lumped together and averaged to yield the final data.

For the graphs, each parameter is plotted against the drawn transistor length. And, only the average (mean) value of the parameter is plotted for each parameter.

Test Chip: BATGIRL  
Fab Name: xxxxx  
Process Name: A2  
Substrate Type: P-type  
Design Rule DB: A2 (min poly = 0.24um)  
Device Size Bias: Wbias=0.0um, Lbias(N)=0.0um, Lbias(P)=0.0um  
Lot Number: CYS18T02  
Test Wafer ID: S6LPGUT, SWLPK2T & SNLPKAT  
Split Condition: None  
Test Sites/Wafer: 9 sites per wafer  
Test Equipment: HP4062UX Parametric Test System #2  
Test Software: "C8 PCM Testing, rev 1.1", May 1992, by Fred Wahl

- **Summary of results:**

The following table summarizes the list of electrical parameters characterized in this report.

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This report is based on a T1 qual lot. A similar report with an extended study will be published on the T2 qual lot.

No unusual behavior is noticed on any parameter. The nominal channel length & the poly design min are both noted on the graphs. The Delta L is calculated using the 3-point method: 2 REF devices and the DUT. The saturated Vt for the zvt device is negative. The Gamma values for the zvt device is quite low. Note that two different off-state leakage current graphs are produced. The only difference between these two is the applied gate voltage - one at 0v & the other at 0.3v.

Additionally, several ‘snapshot’ curves are included in this report. A ‘snapshot’ is a set of 4 graphs (Id-Vg-Vb (linear), Id-Vd-Vg, Id-Vg-Vb (sub-threshold) and Rout-Vd) from a single bench measurement using the BTA BSimPro Software. There are 4 ‘snapshots’ for NFET (20/0.24, 15/0.24, 1/2 & 1/0.24), 4 for PFET (15/0.24, 15/2, 1/2, 1/0.24) & 4 for ZeroVt FET (15/0.46, 15/0.56, 15/2 & 2/0.46). Also, several temperature ‘snapshots’ are included: 20/0.24 NFET at 130<sup>0</sup>C, 105<sup>0</sup>C, 100<sup>0</sup>C, 75<sup>0</sup>C, 25<sup>0</sup>C, 0<sup>0</sup>C, -40<sup>0</sup>C & -55<sup>0</sup>C, 20/0.24 PFET at 130<sup>0</sup>C, 105<sup>0</sup>C, 100<sup>0</sup>C, 75<sup>0</sup>C, 25<sup>0</sup>C, 0<sup>0</sup>C, -40<sup>0</sup>C & -55<sup>0</sup>C and 15/0.56 ZVT NFET at 130<sup>0</sup>C, 105<sup>0</sup>C, 100<sup>0</sup>C, 75<sup>0</sup>C, 25<sup>0</sup>C, 0<sup>0</sup>C.

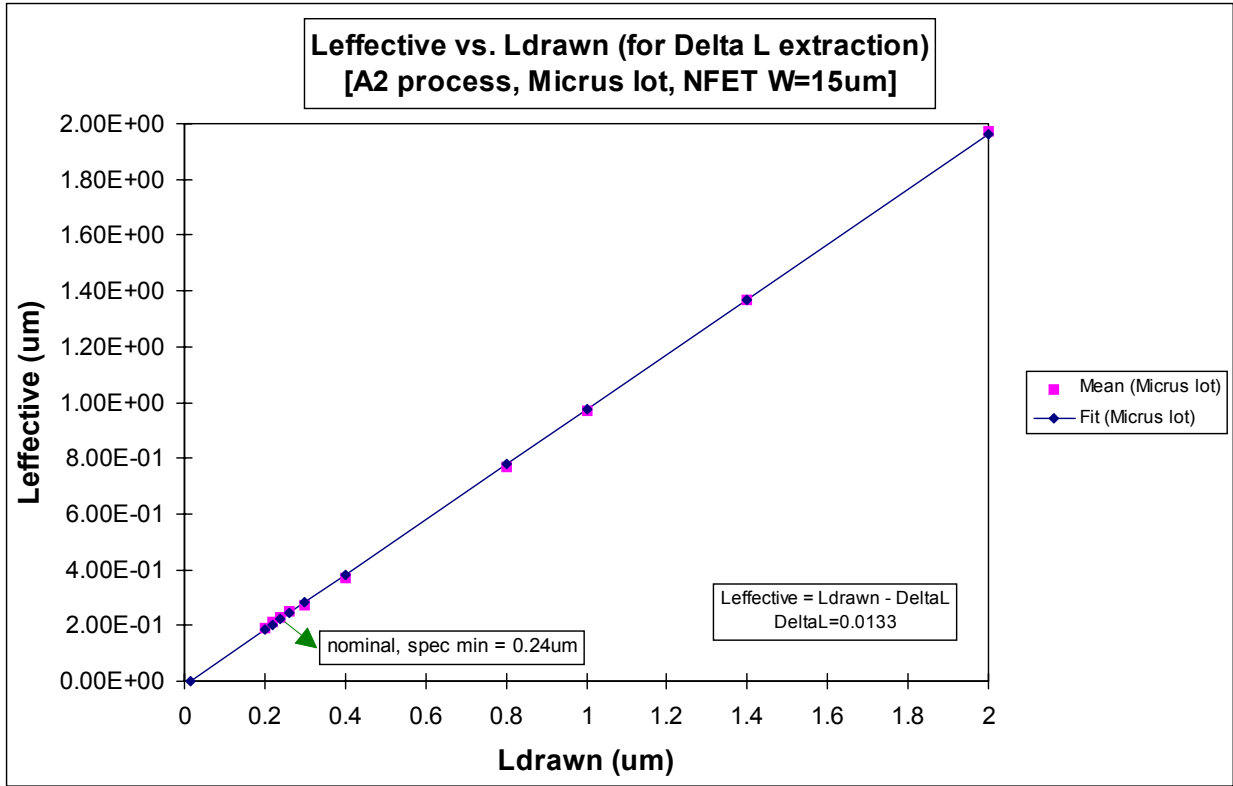


Figure 1

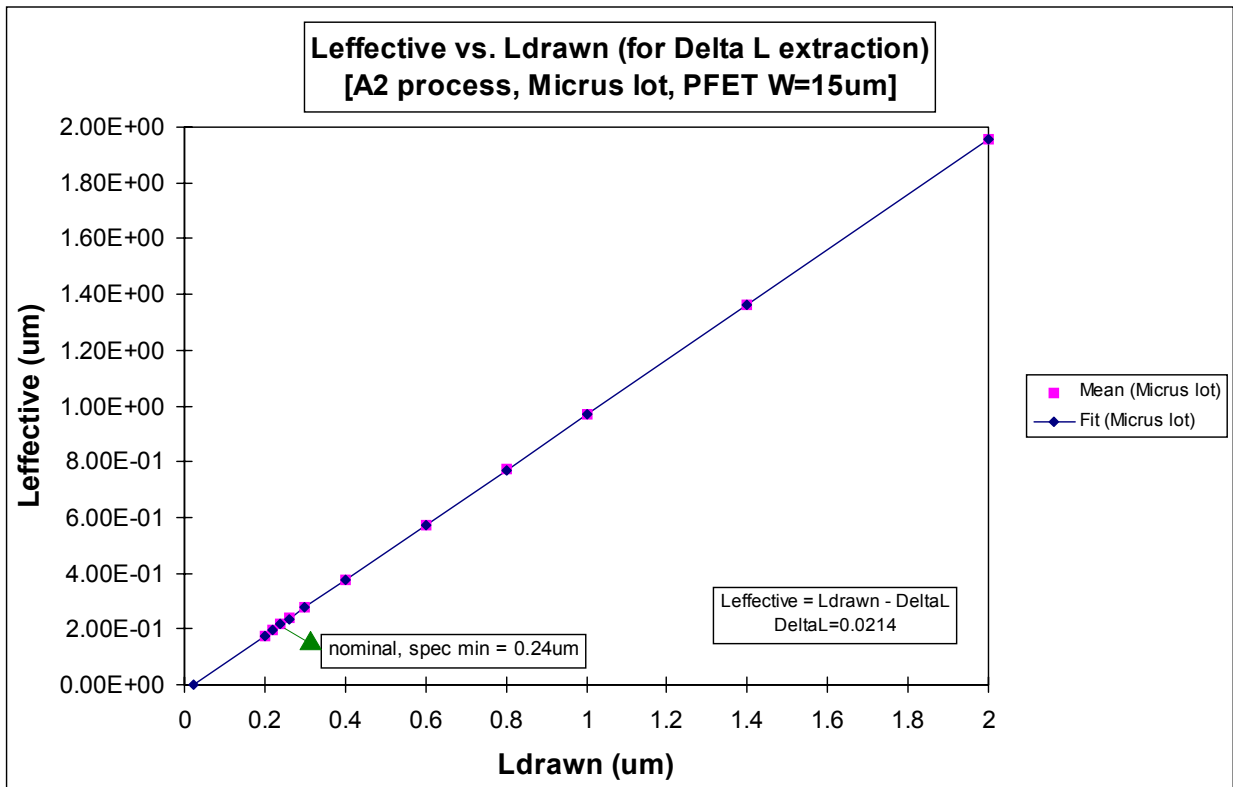


Figure 2

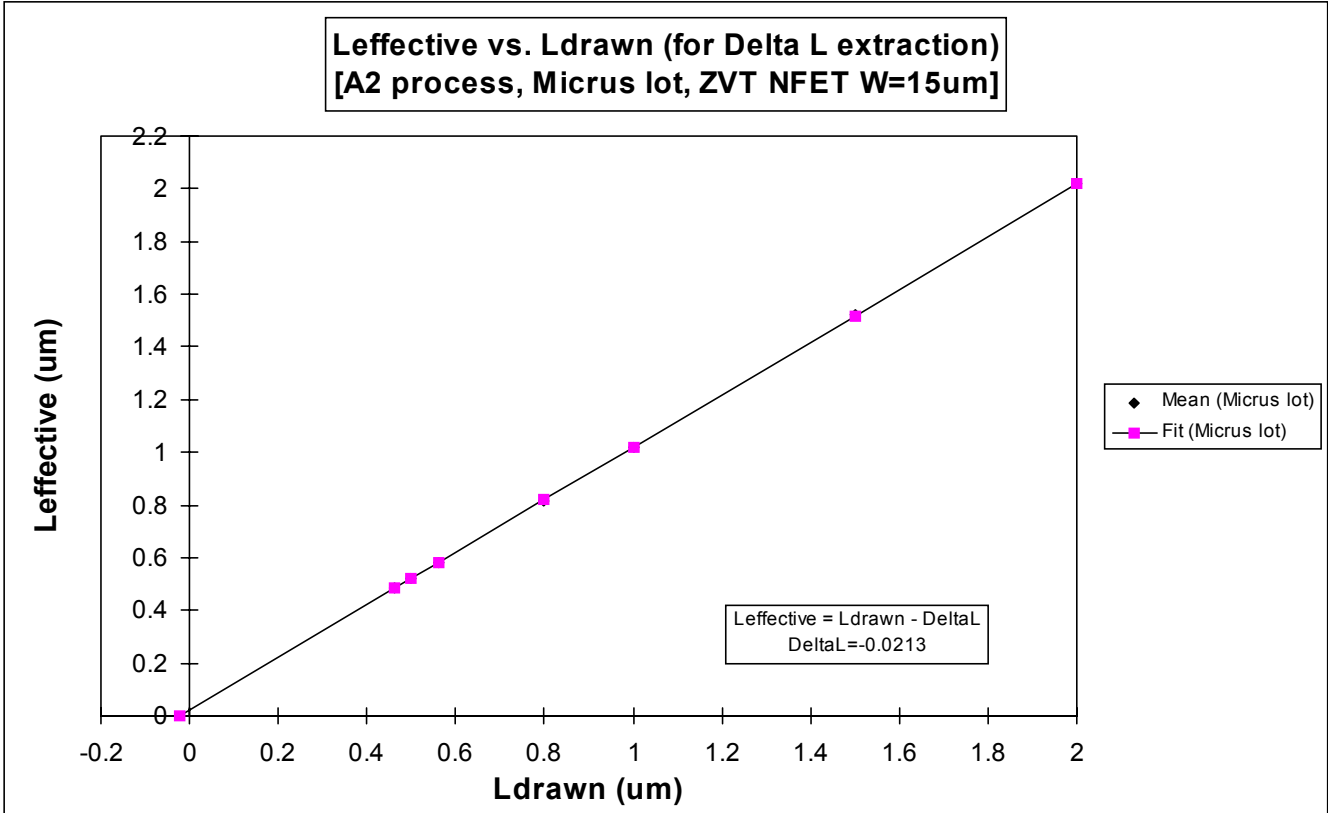


Figure 3

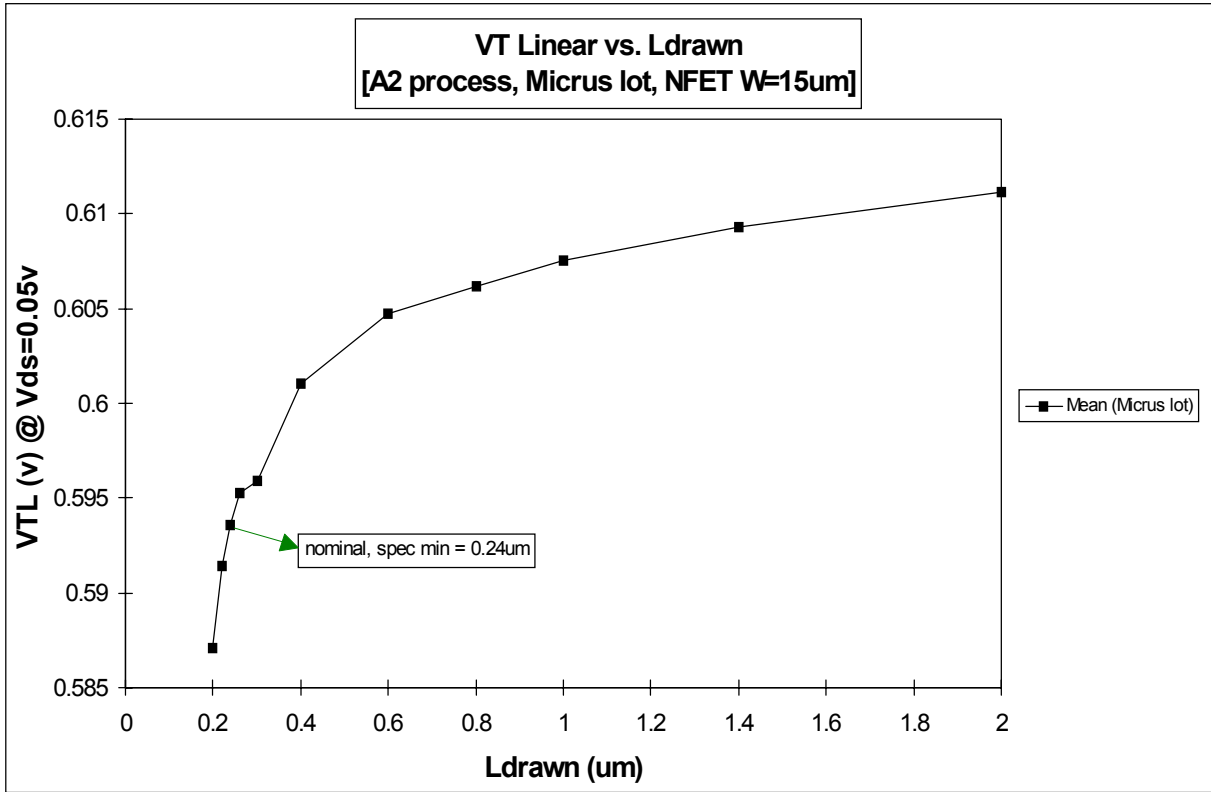


Figure 4

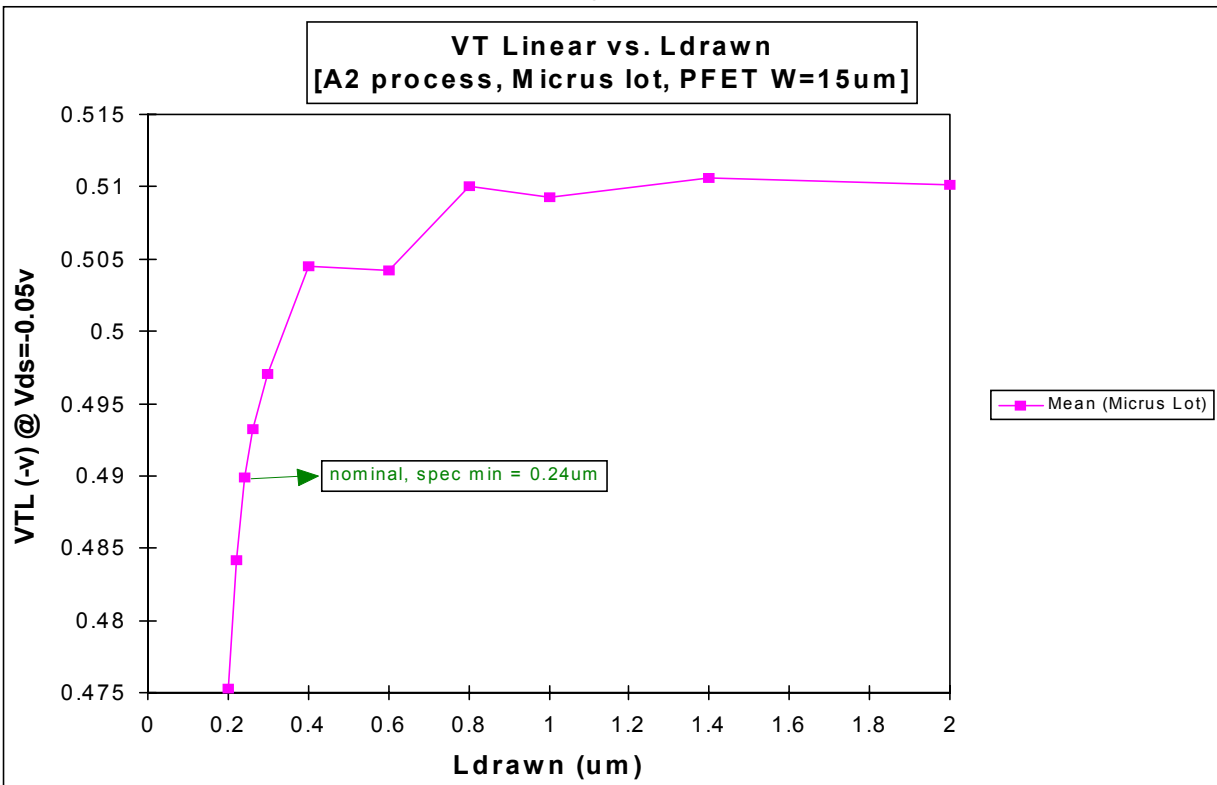


Figure 5

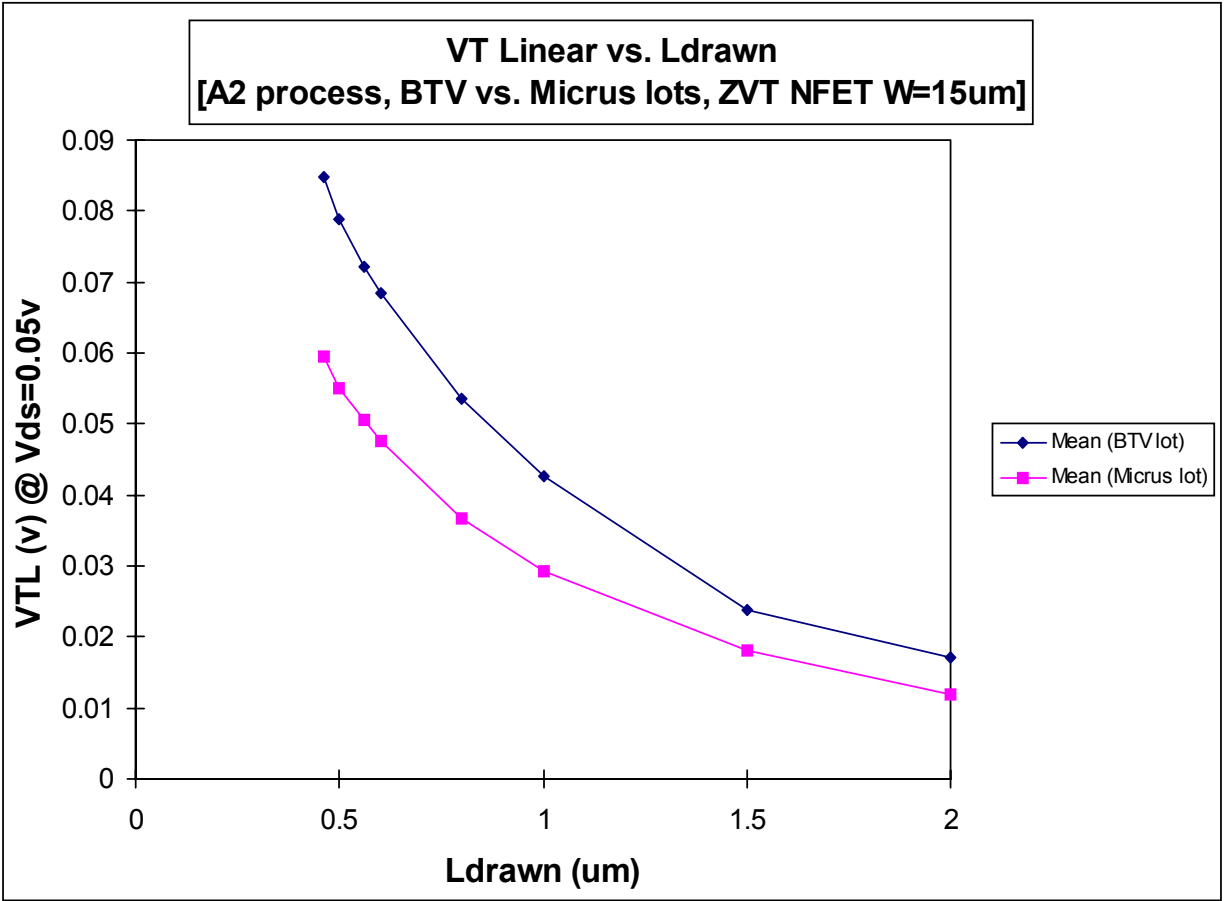


Figure 6

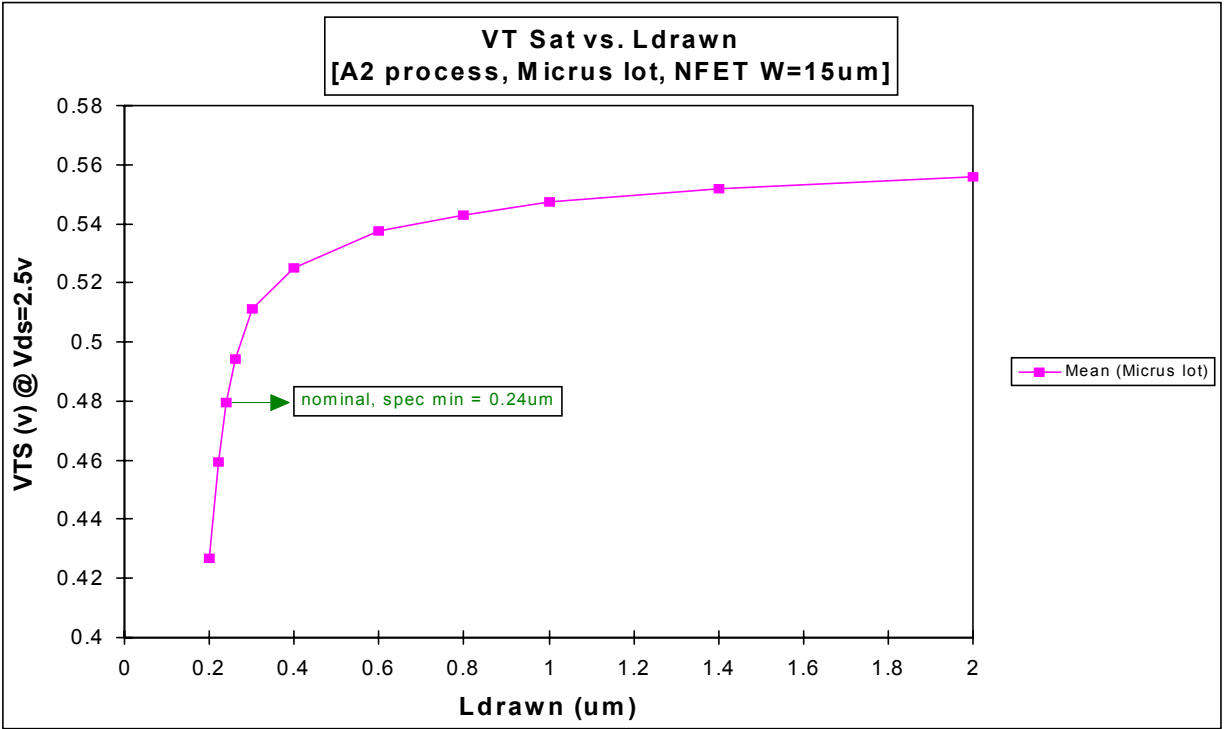


Figure 7

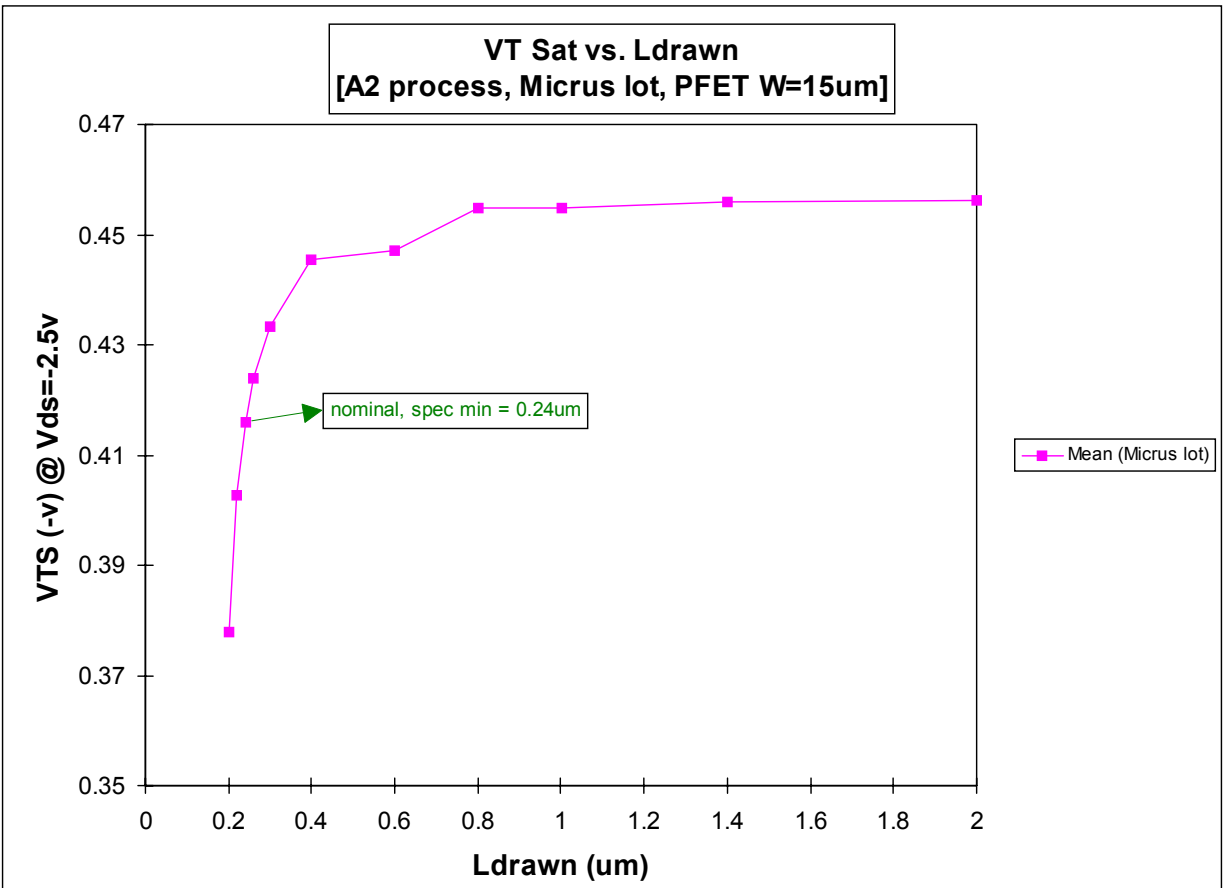


Figure 8

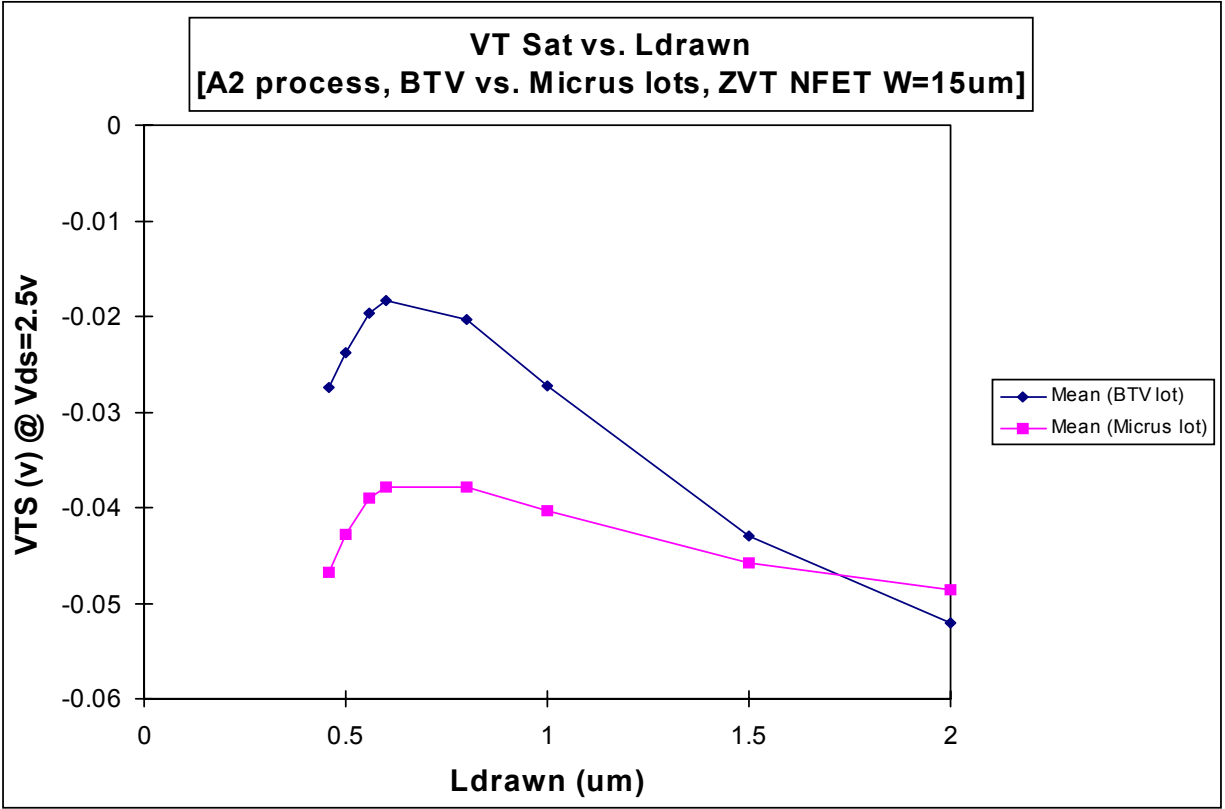


Figure 9

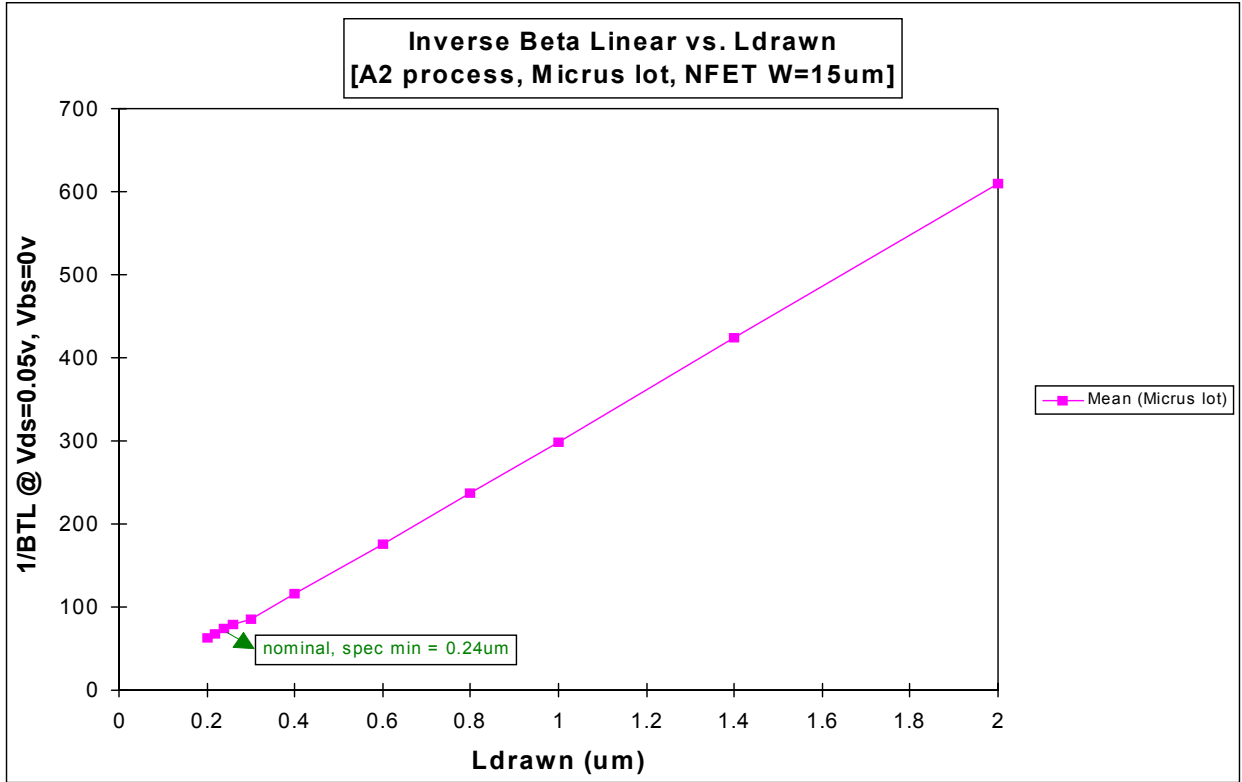


Figure 10

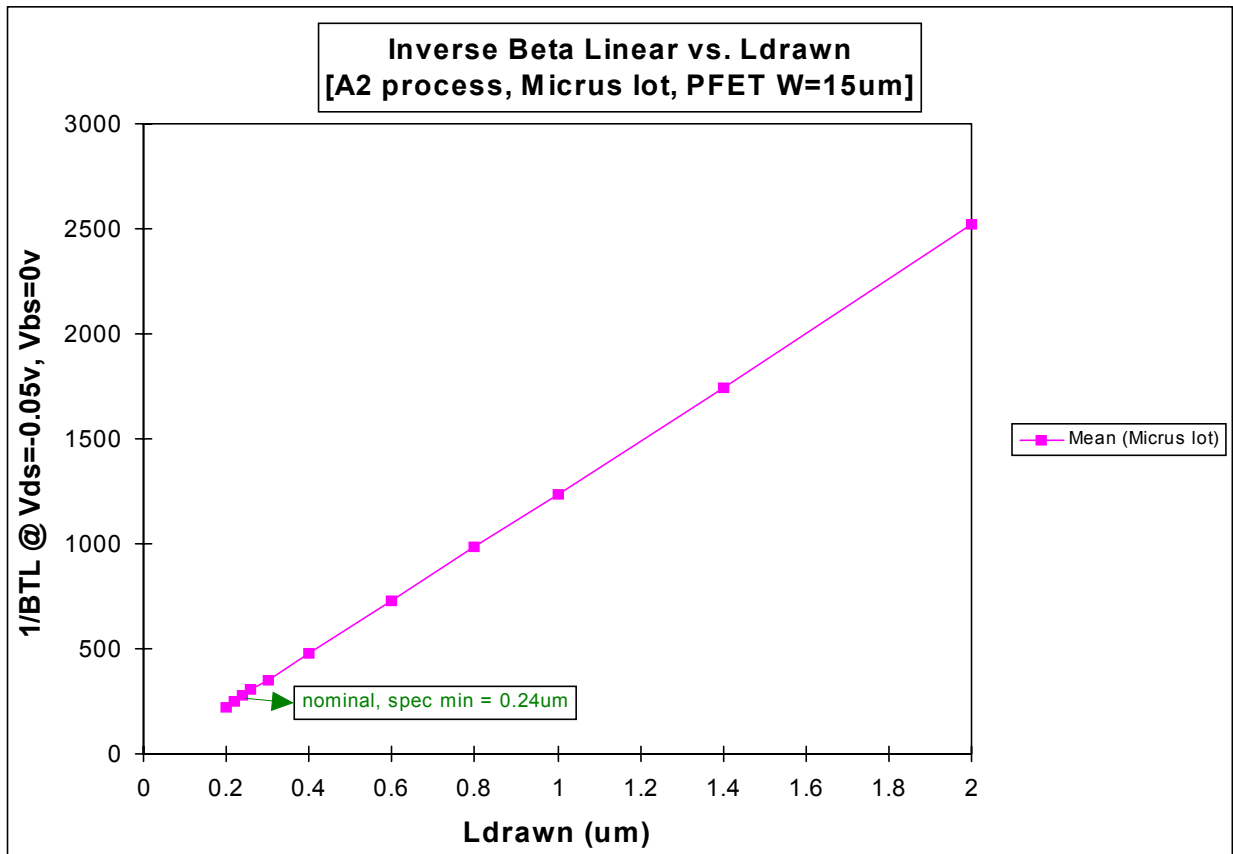


Figure 11

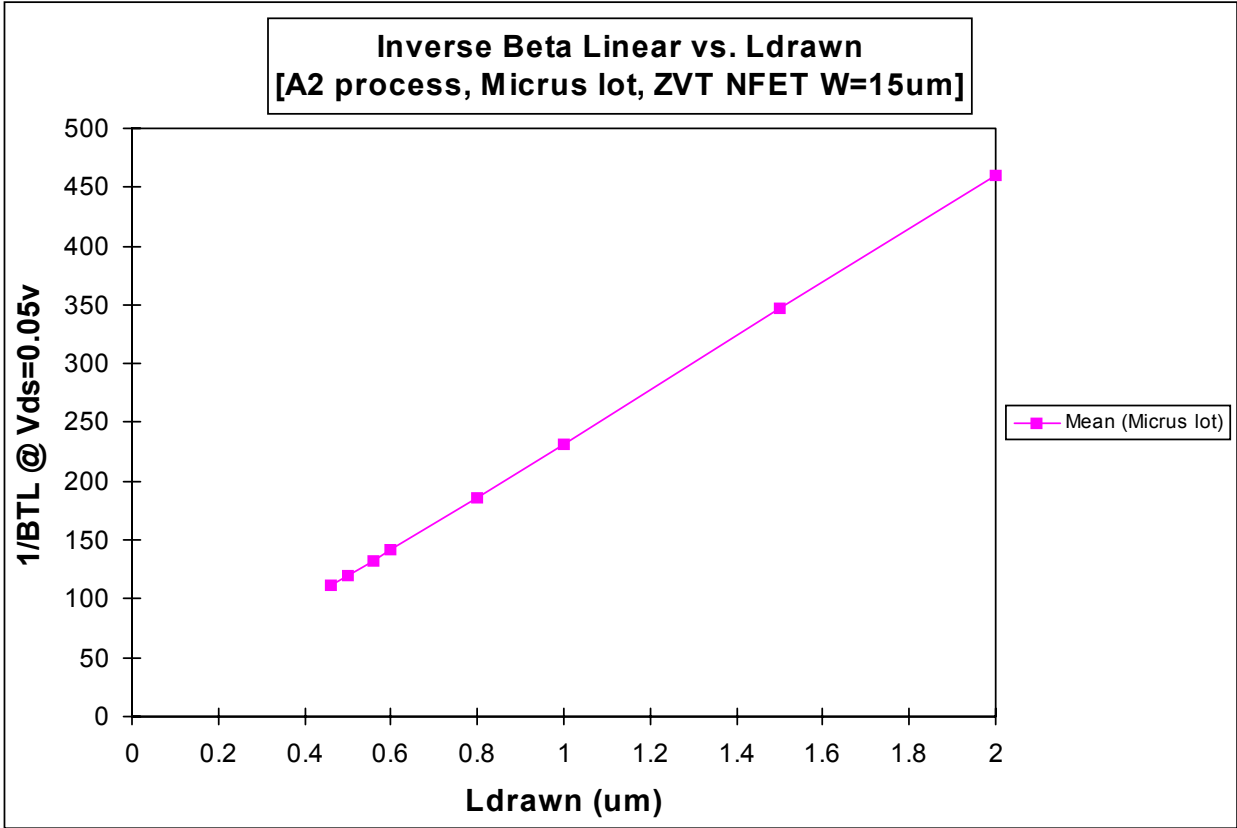


Figure 12

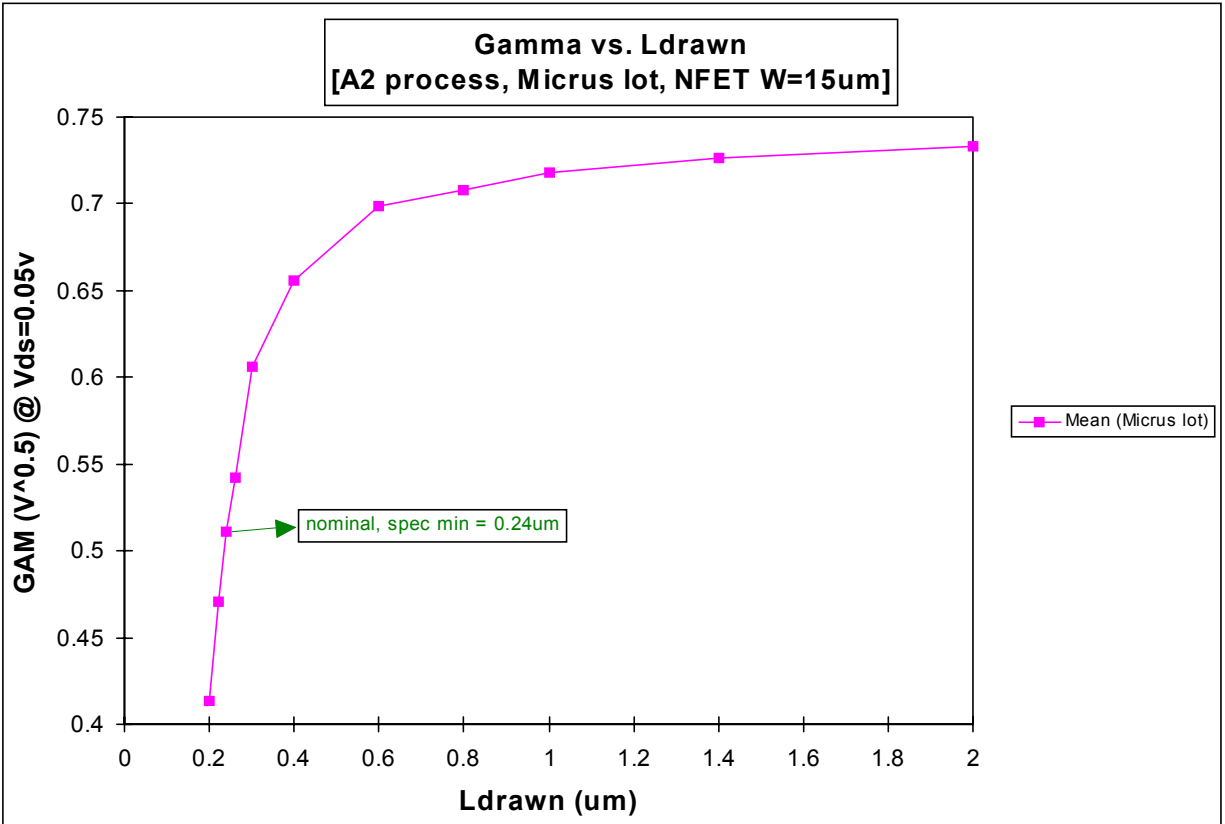


Figure 13

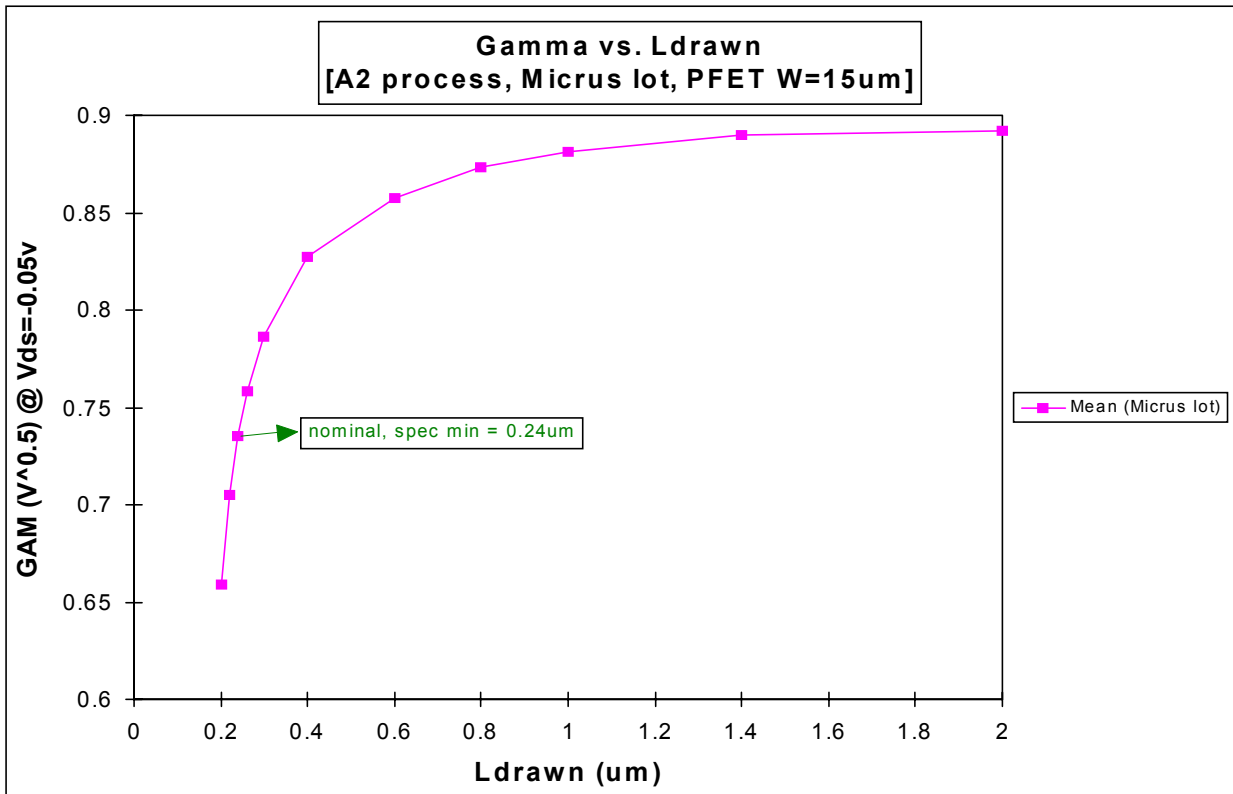


Figure 14

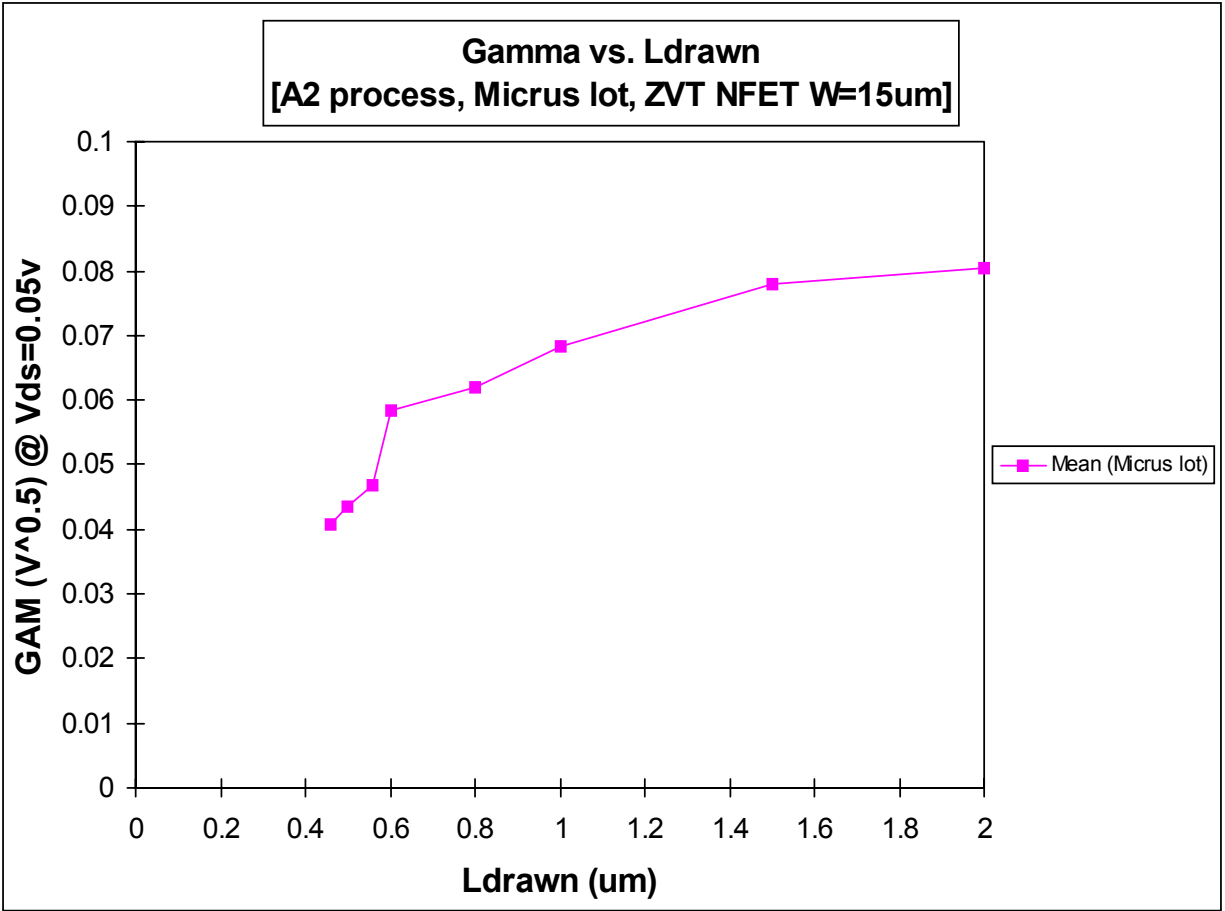


Figure 15

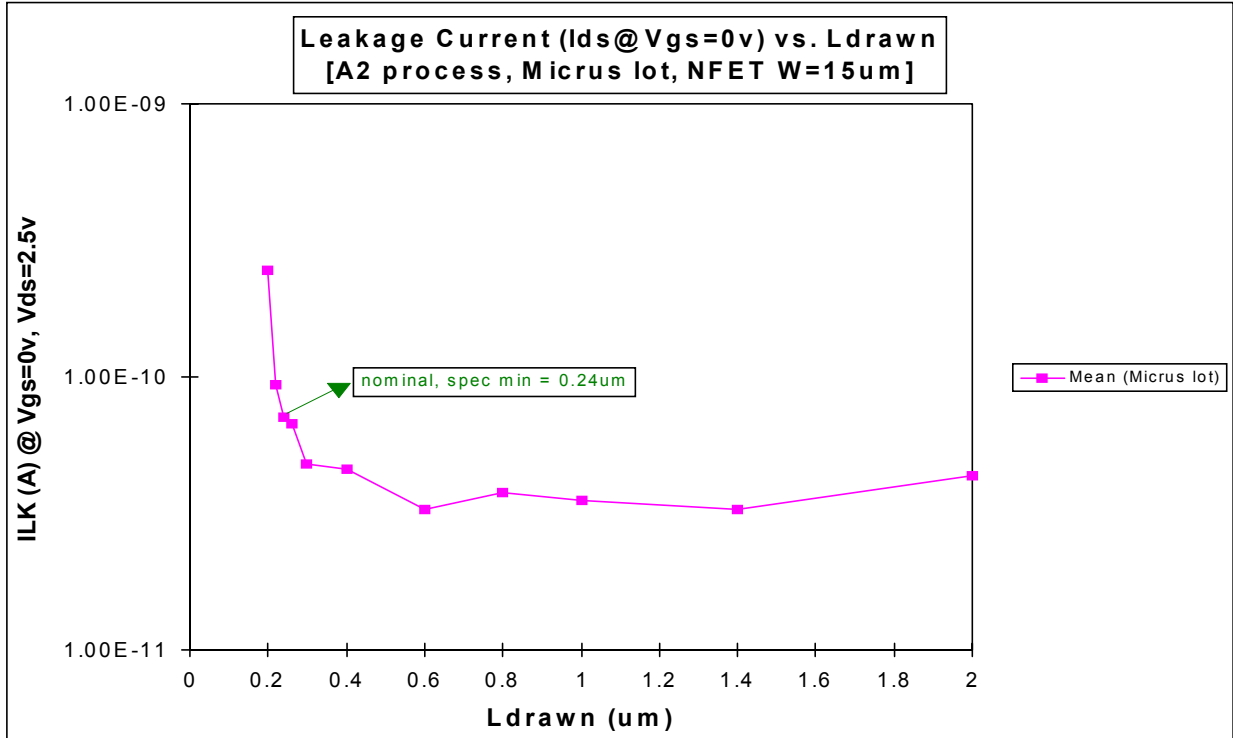


Figure 16

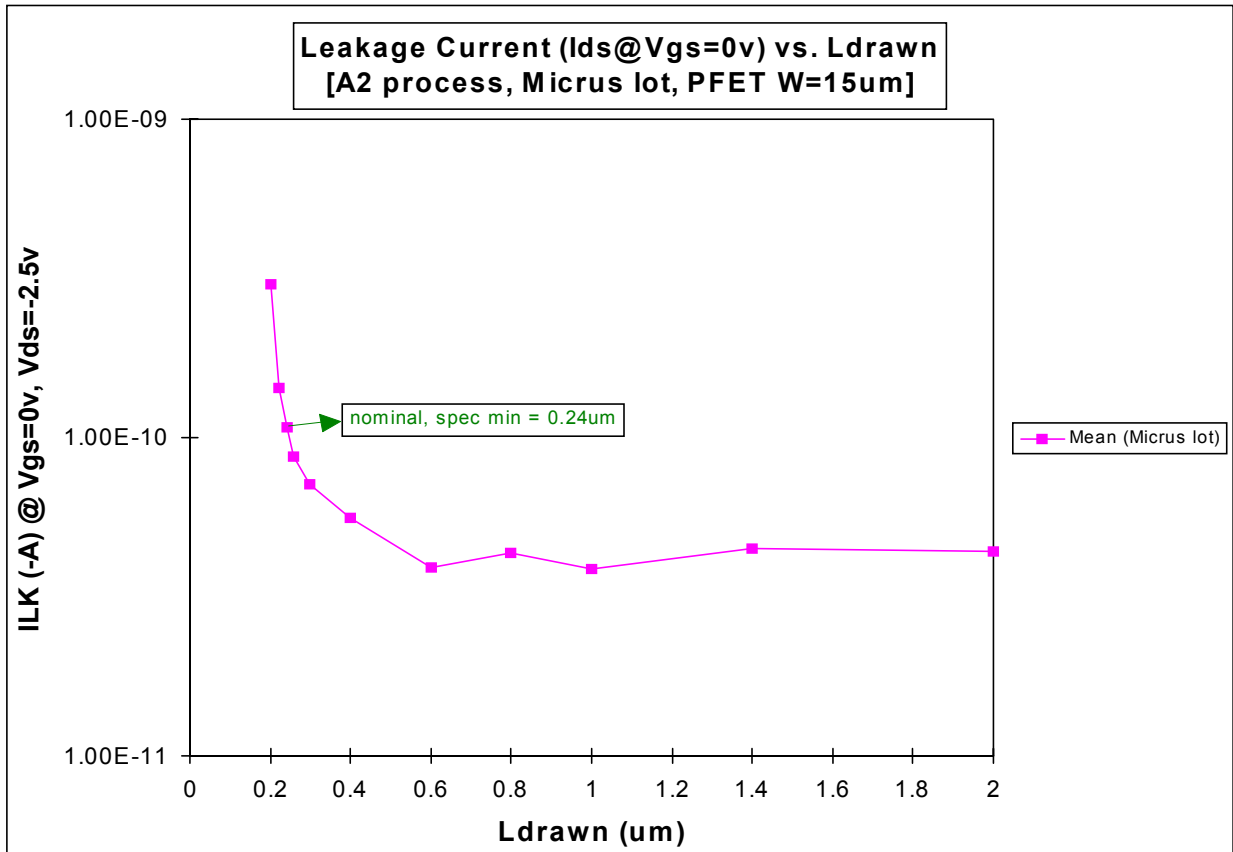


Figure 17

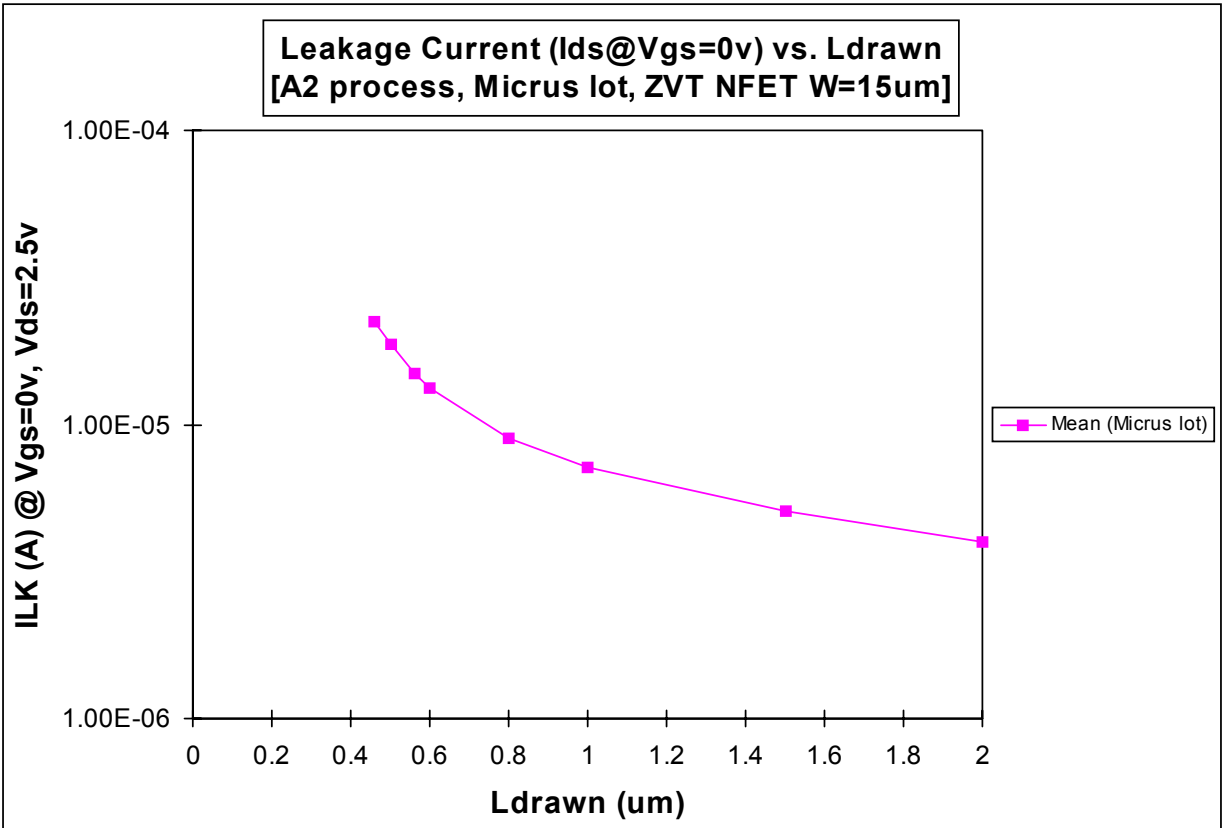


Figure 18

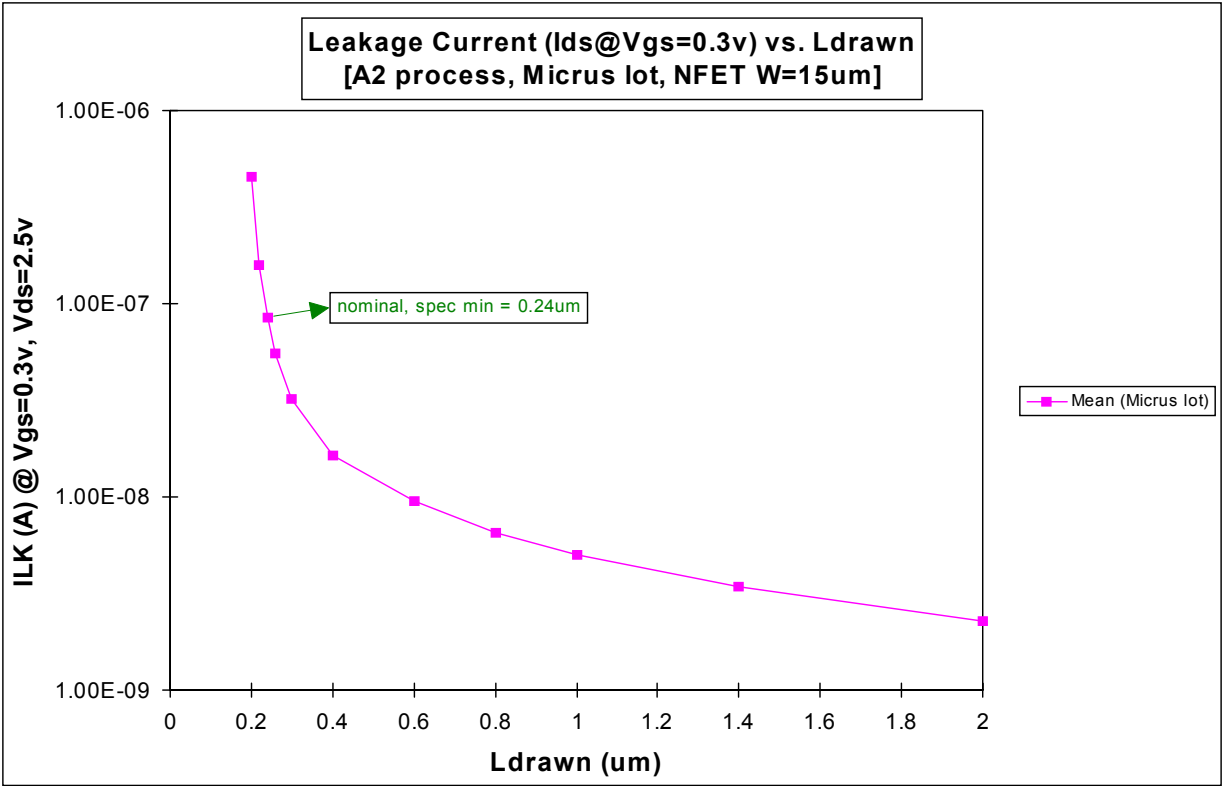


Figure 19

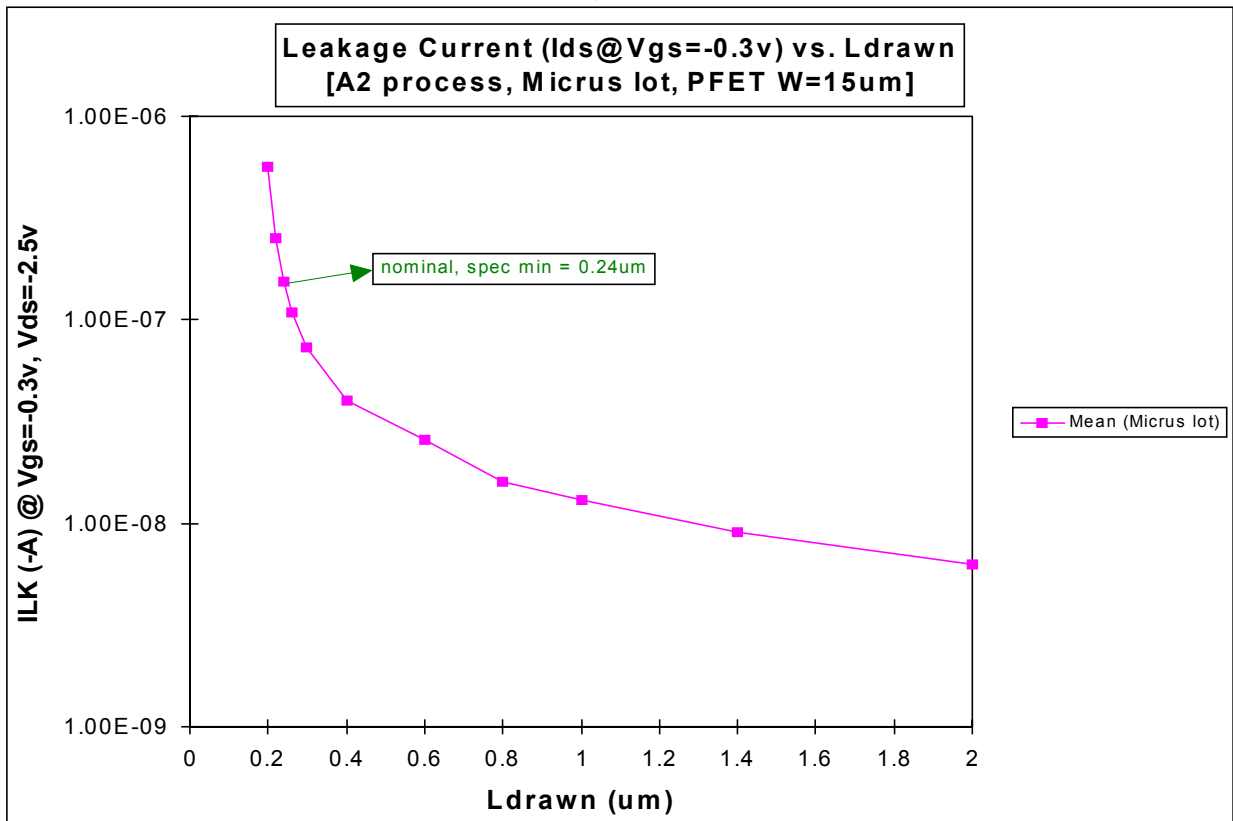


Figure 20

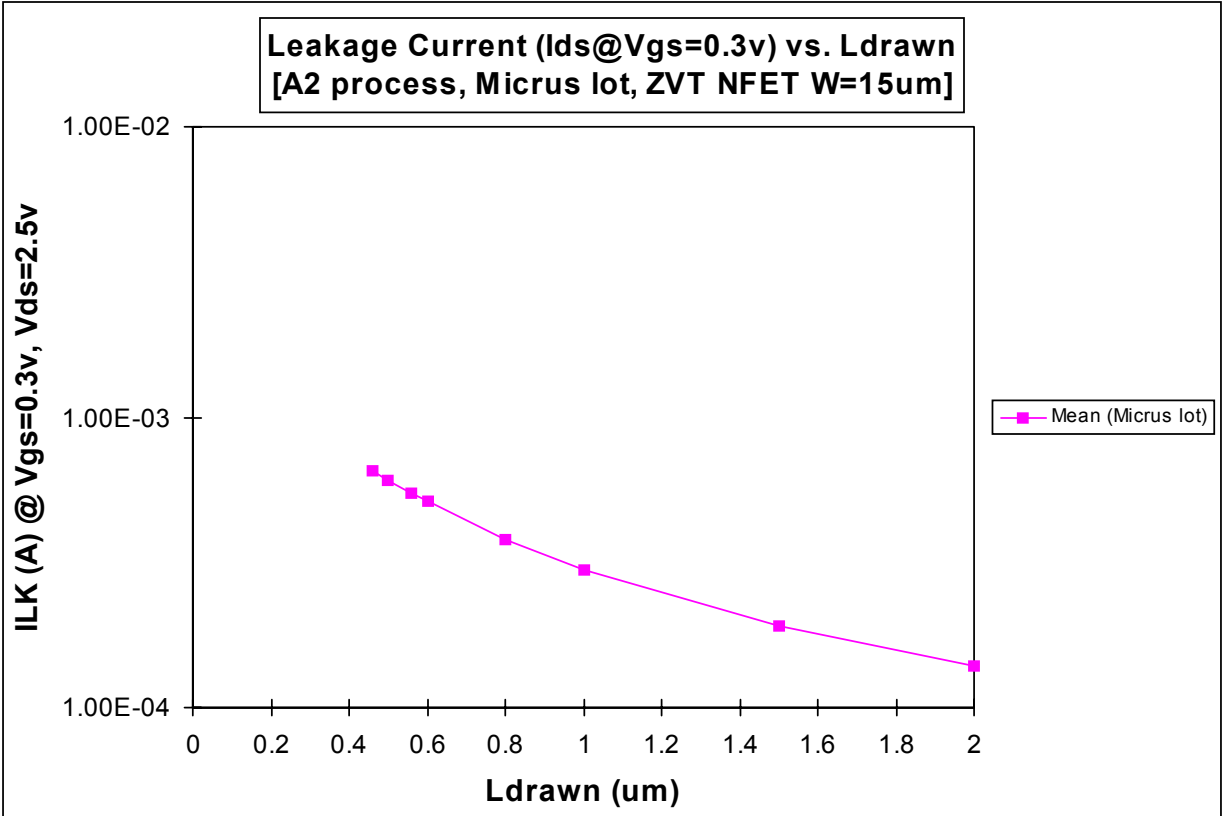


Figure 21

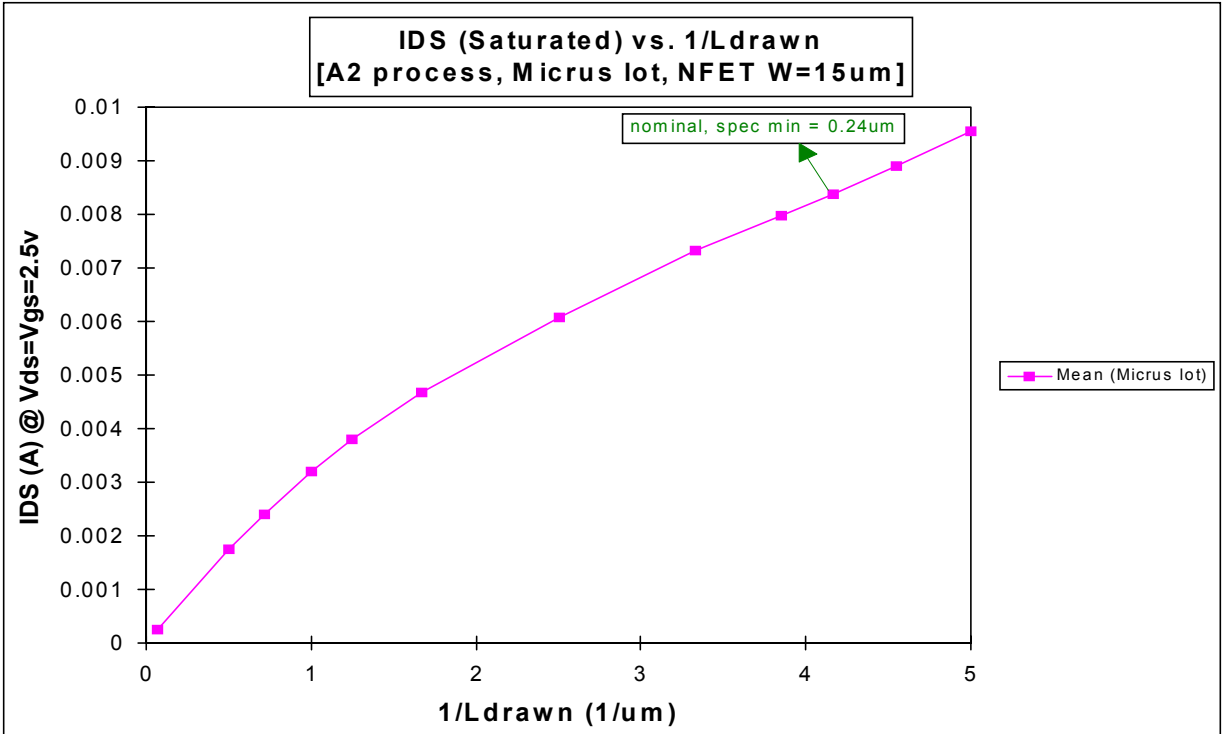


Figure 22

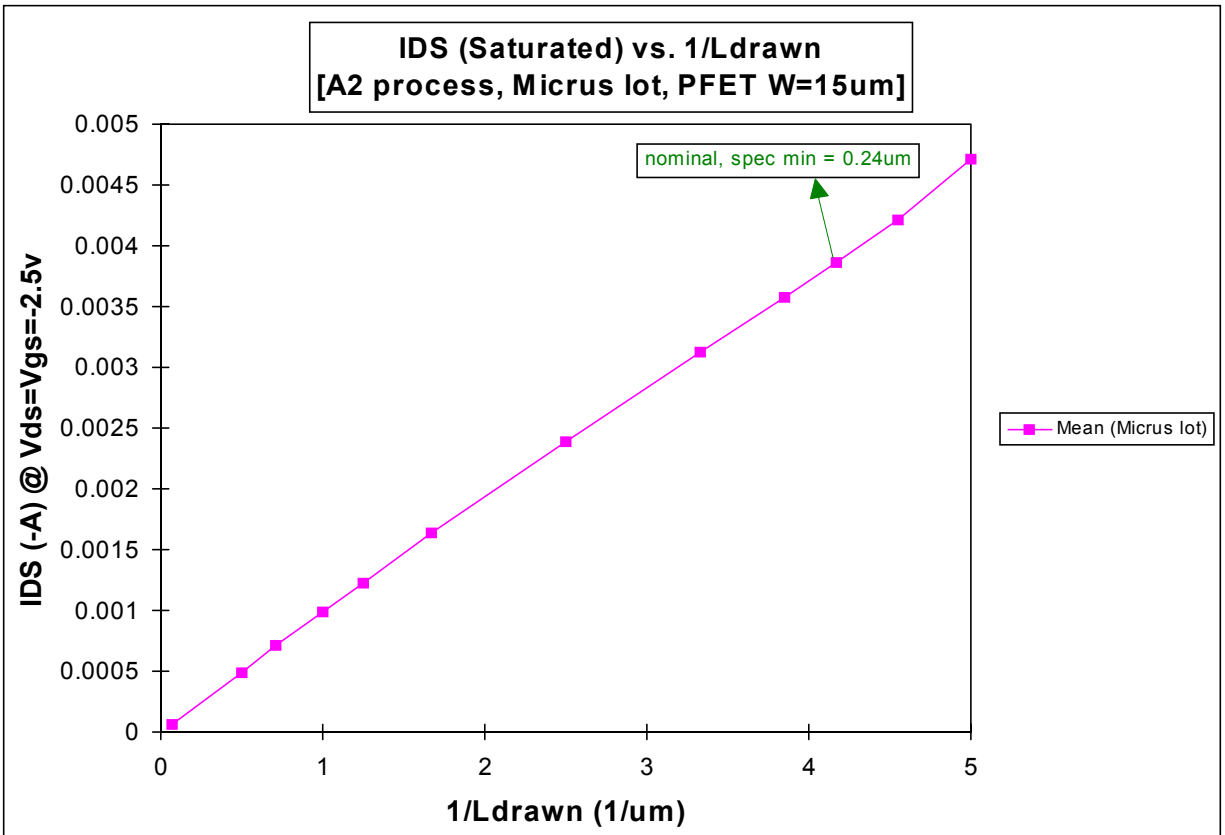


Figure 23

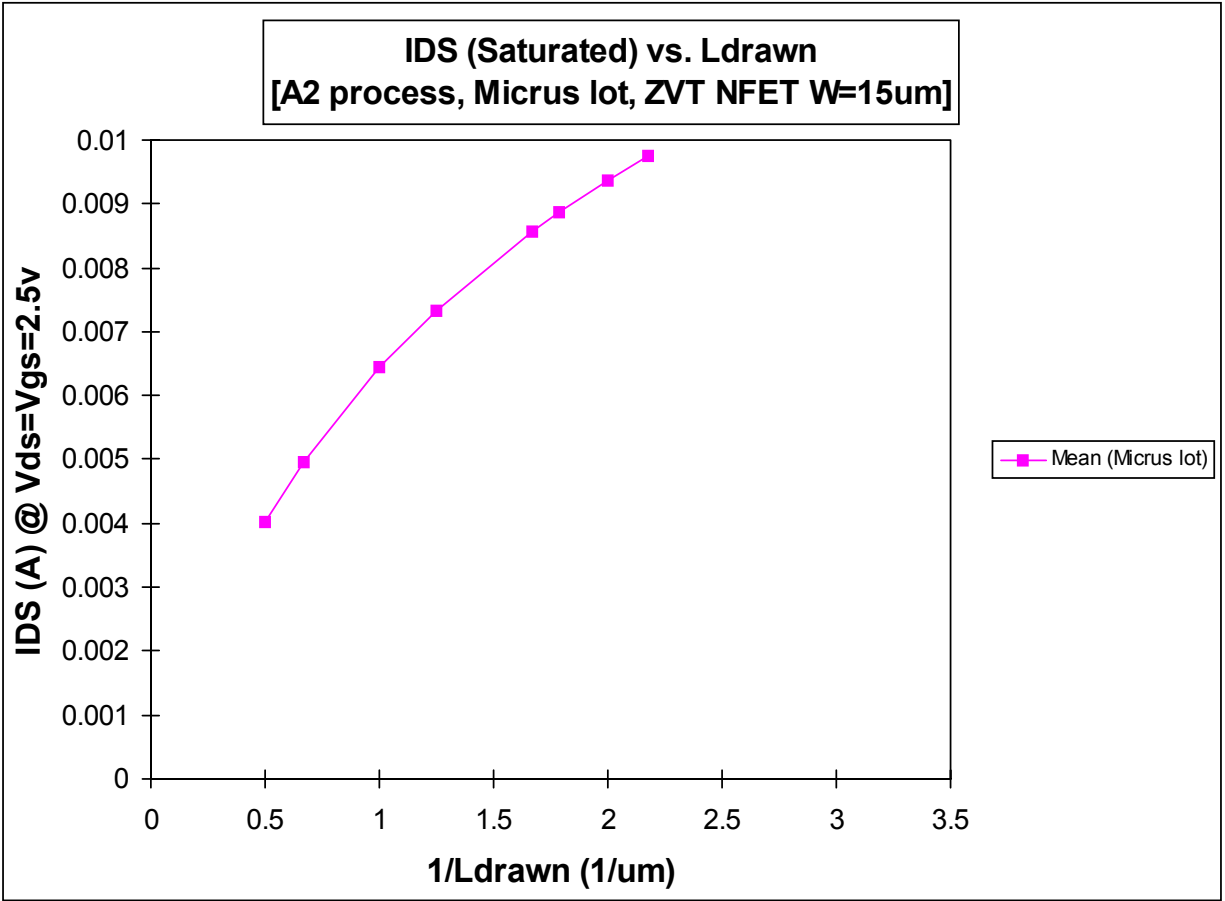


Figure 24

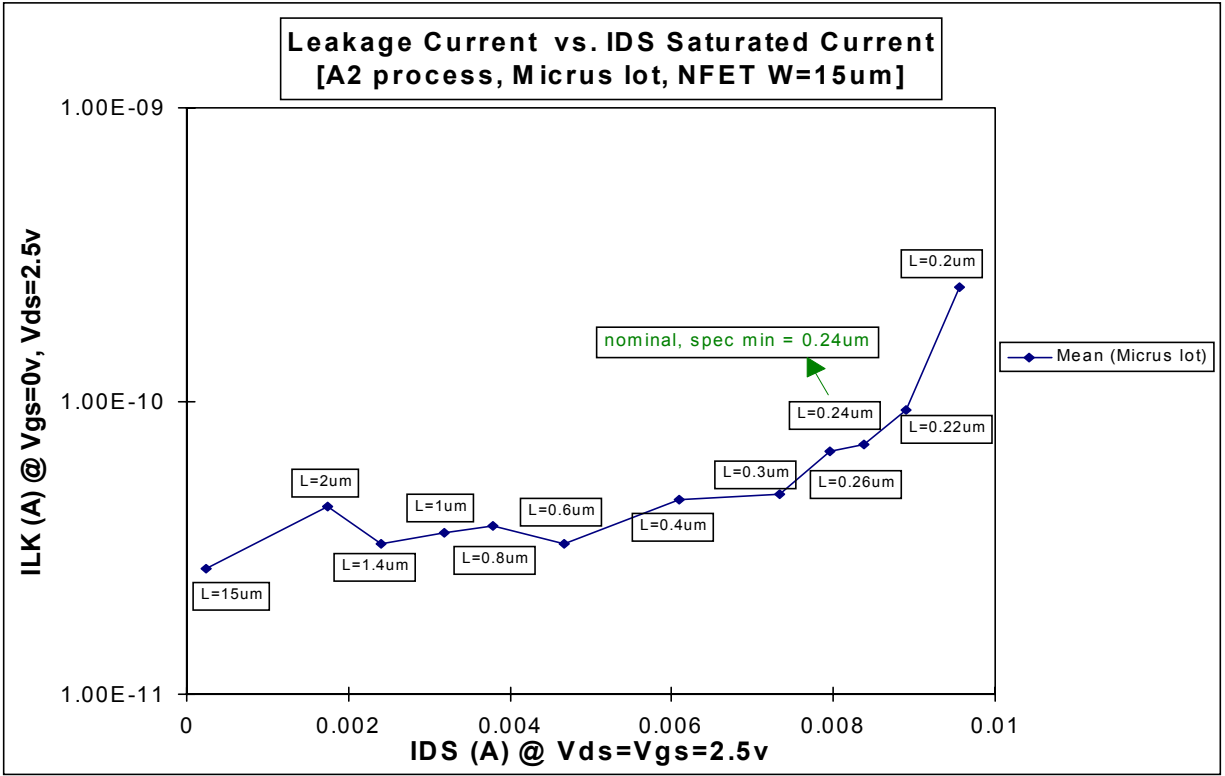


Figure 25

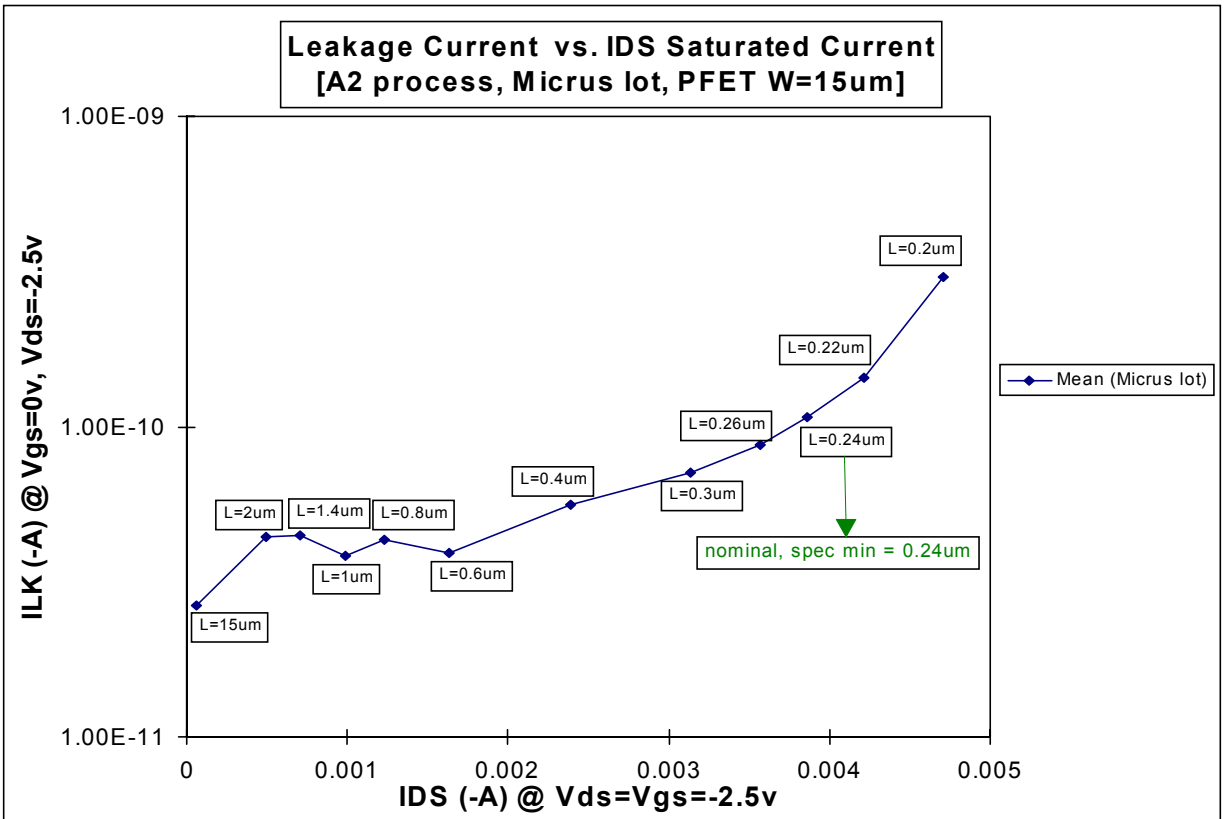


Figure 26

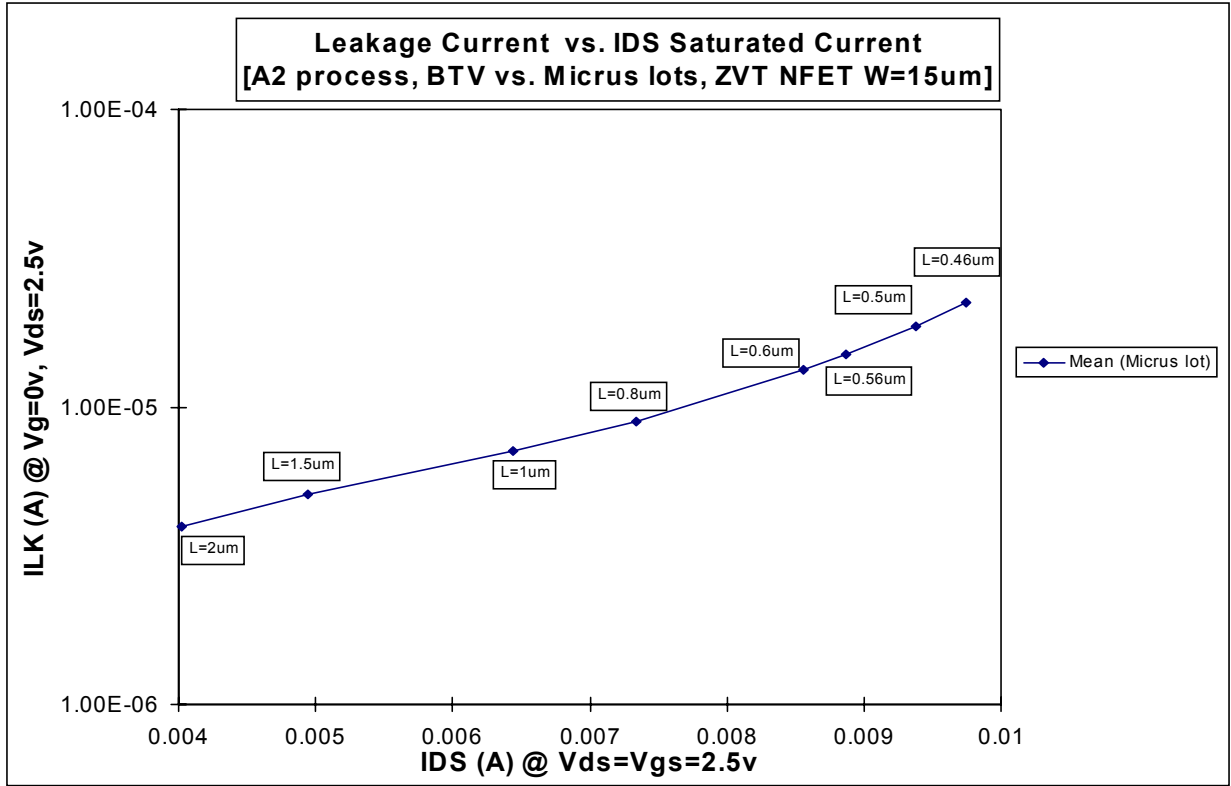


Figure 27

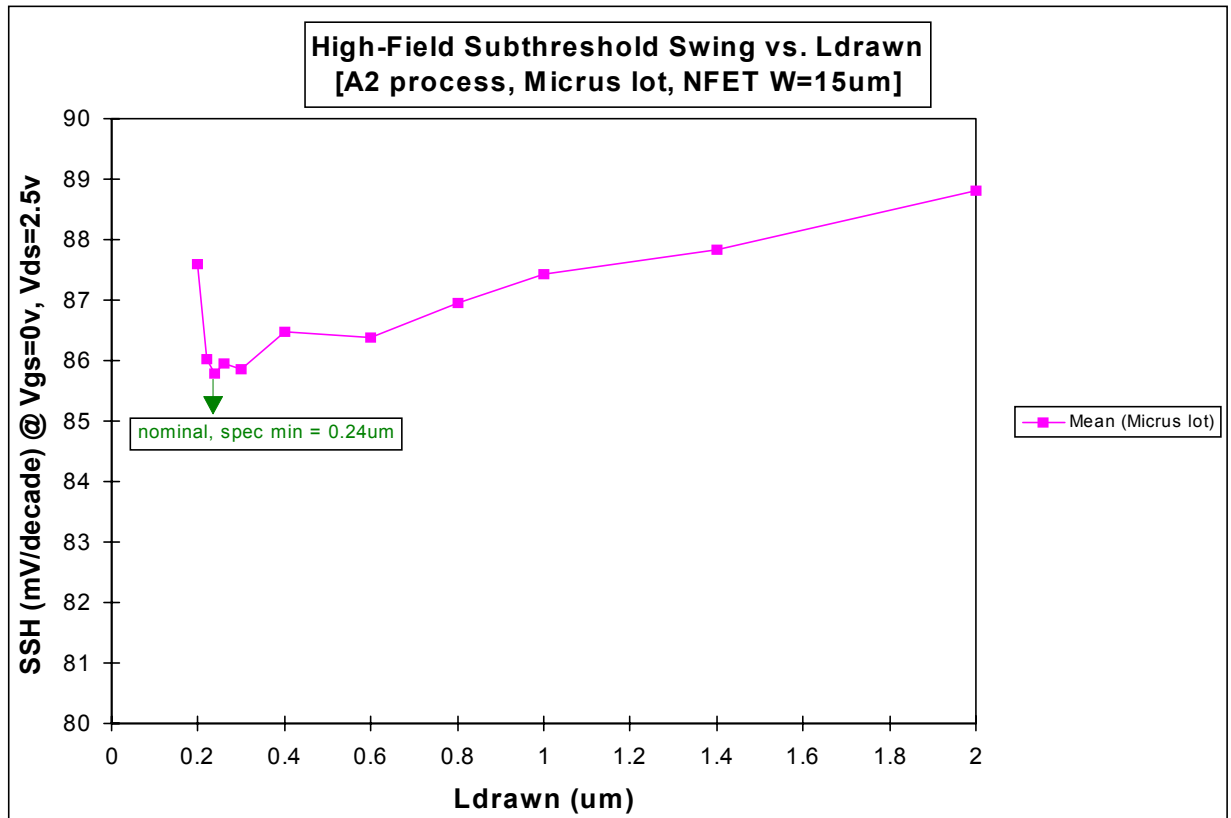


Figure 28

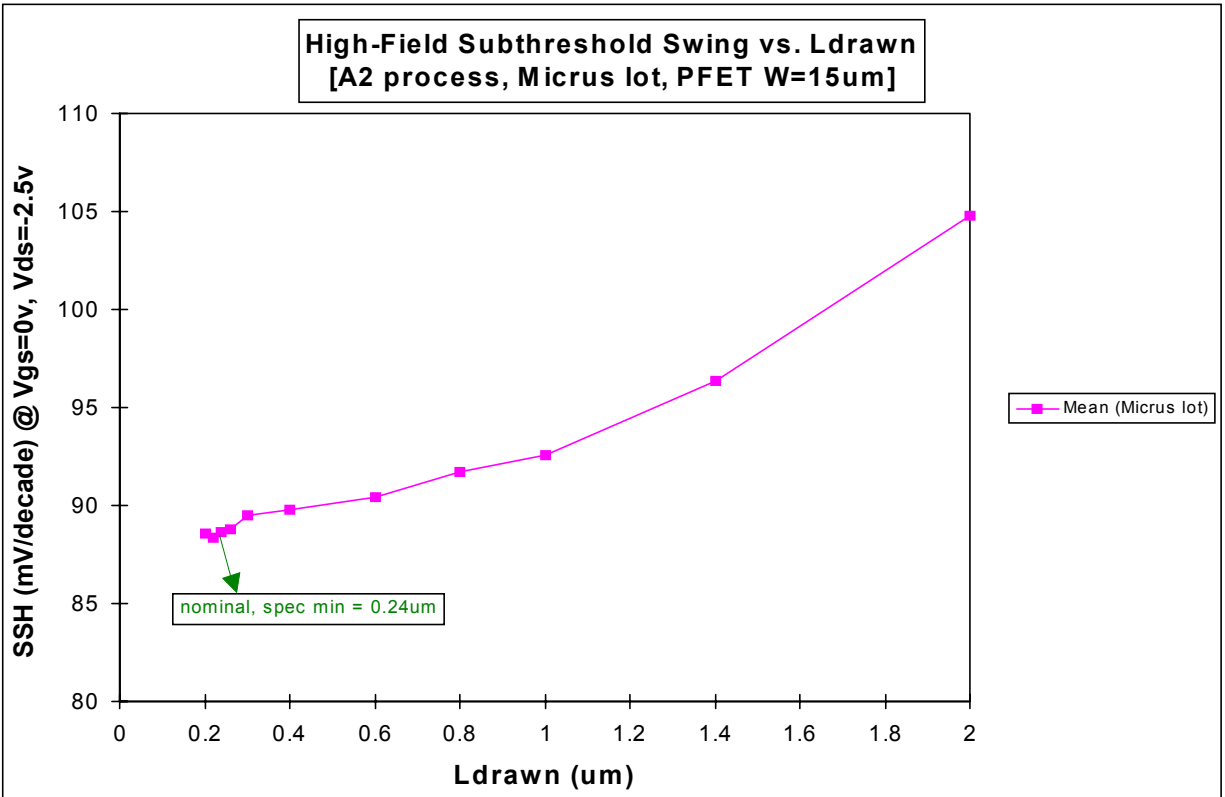


Figure 29

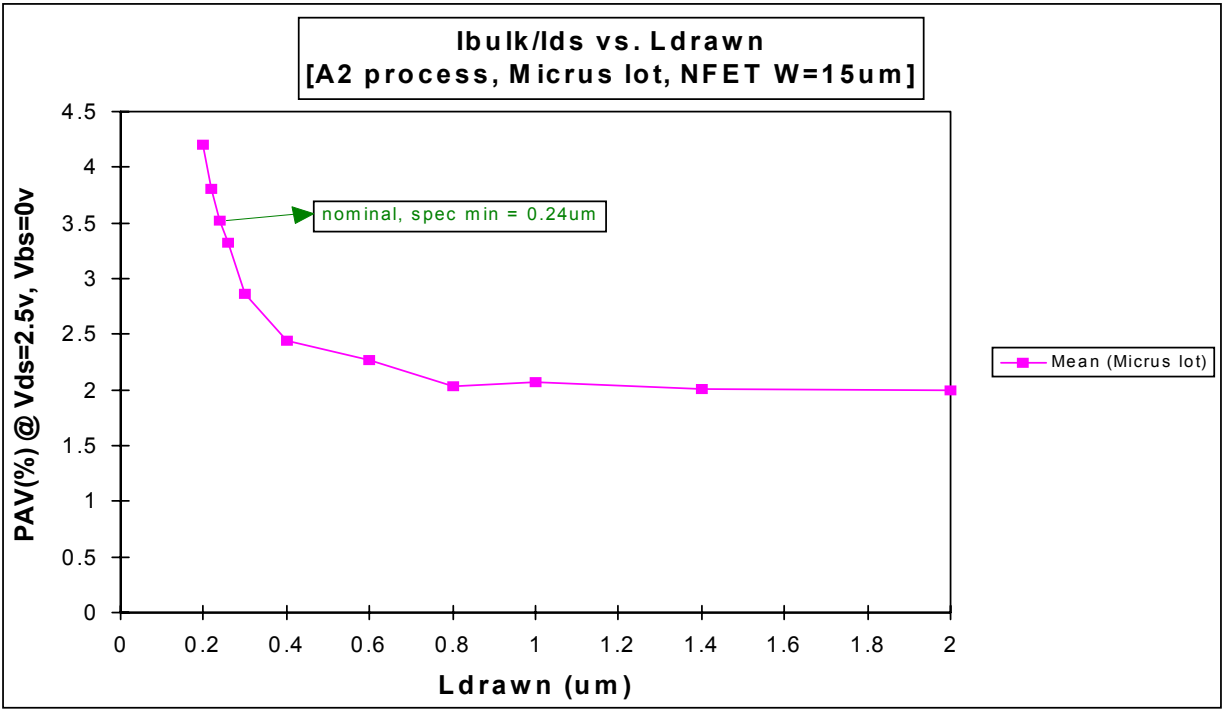


Figure 30

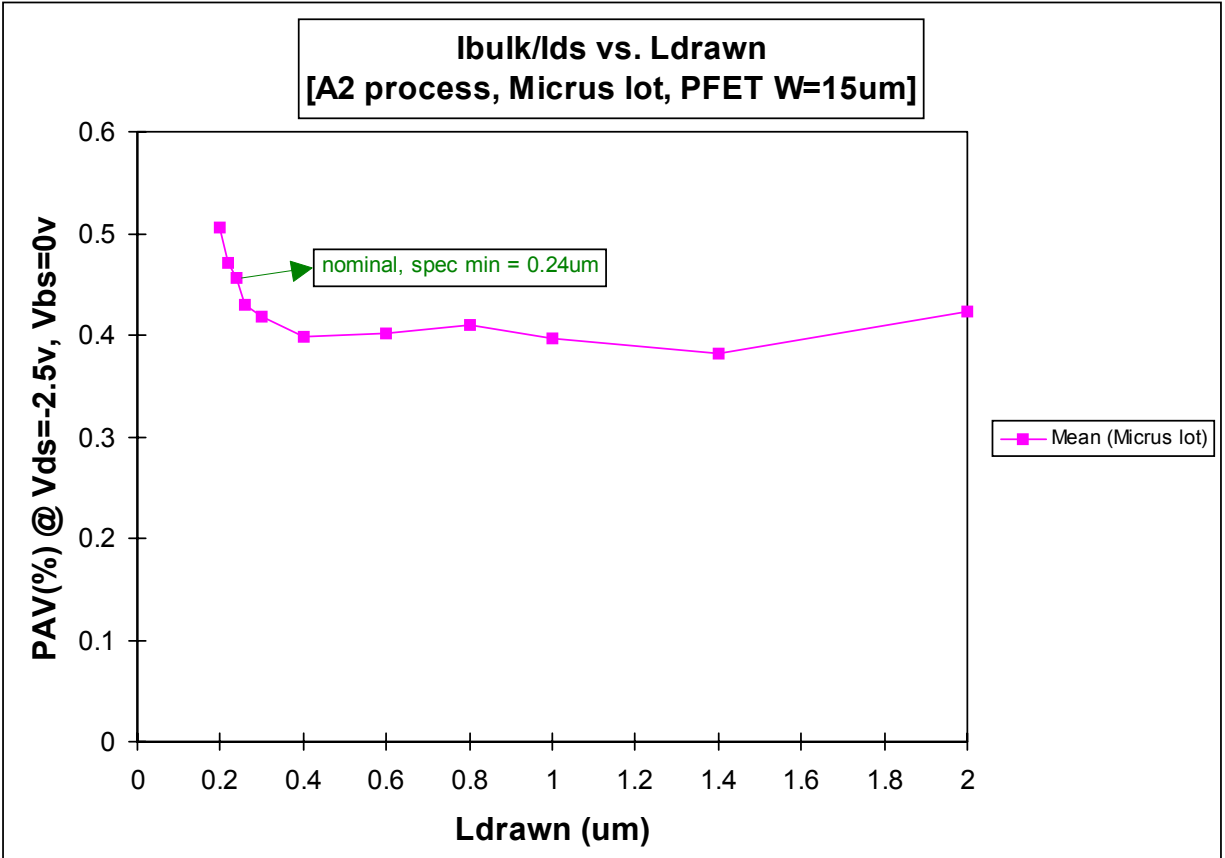


Figure 31

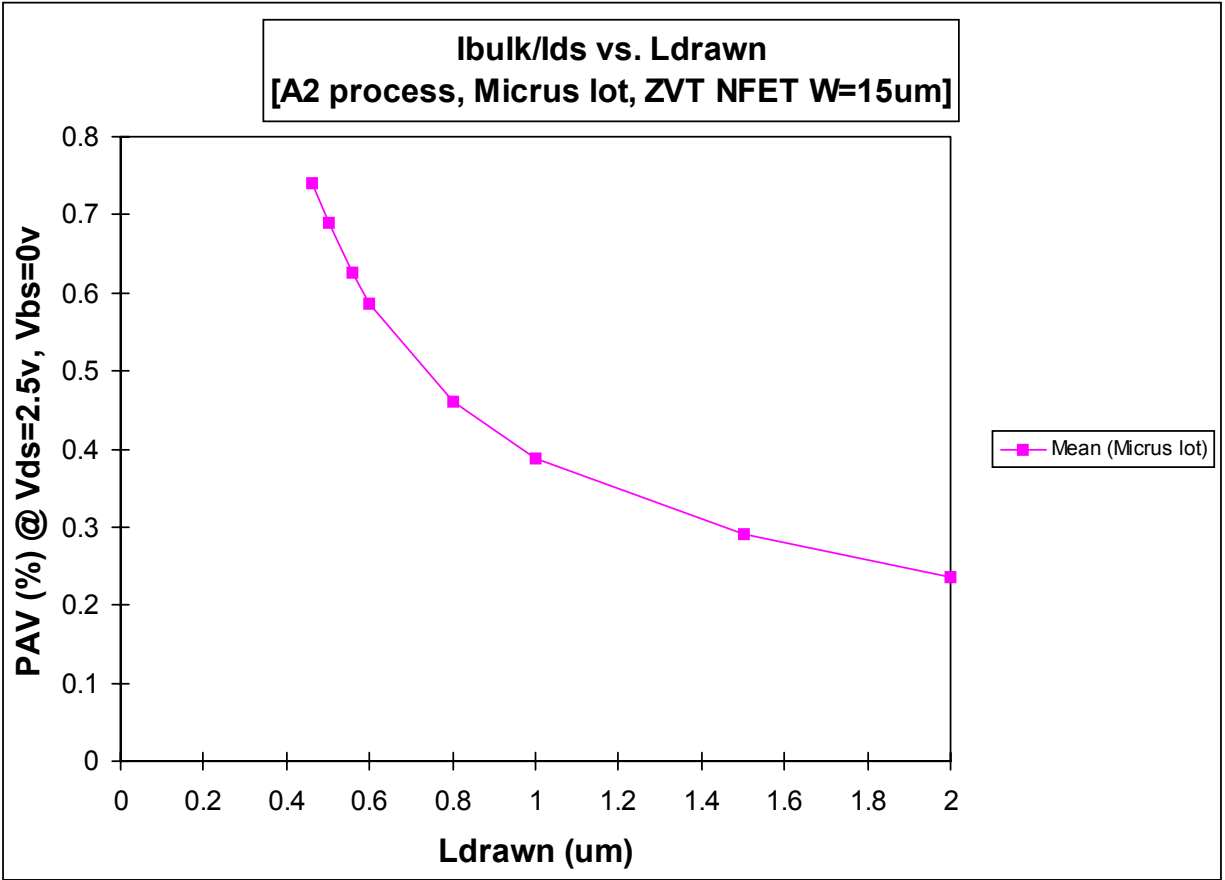


Figure 32

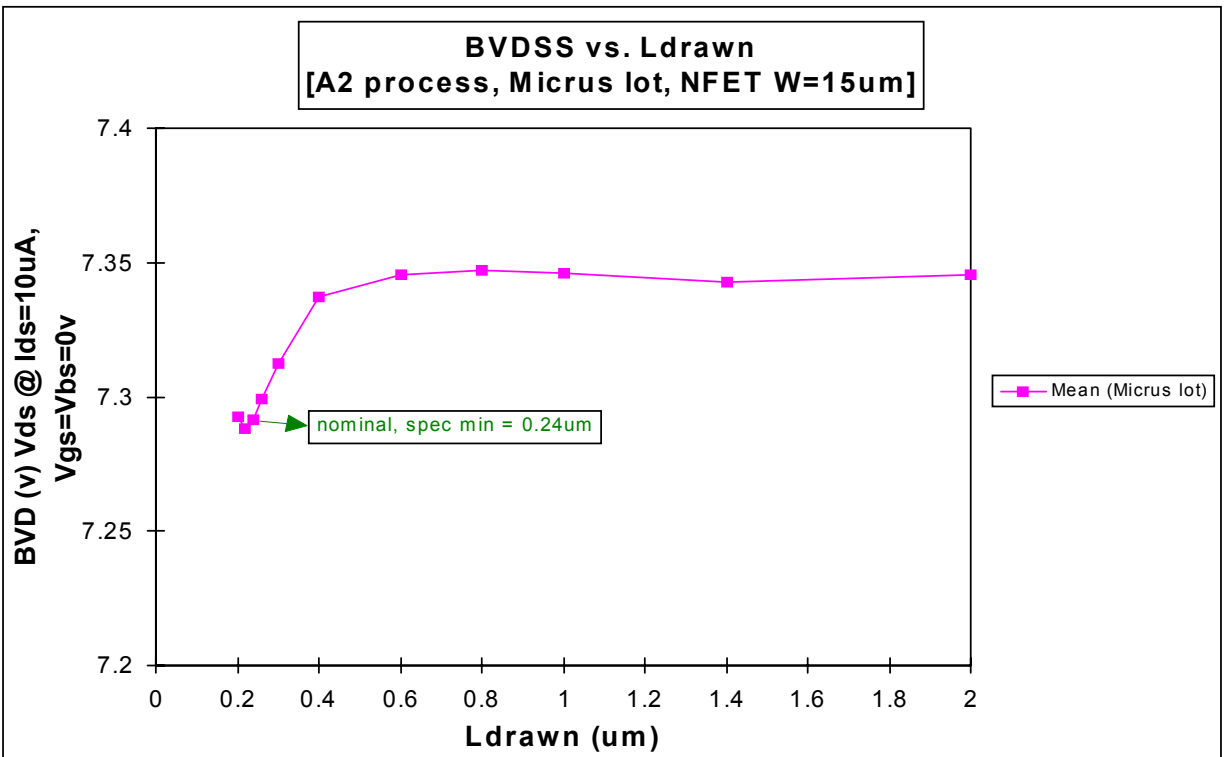


Figure 33

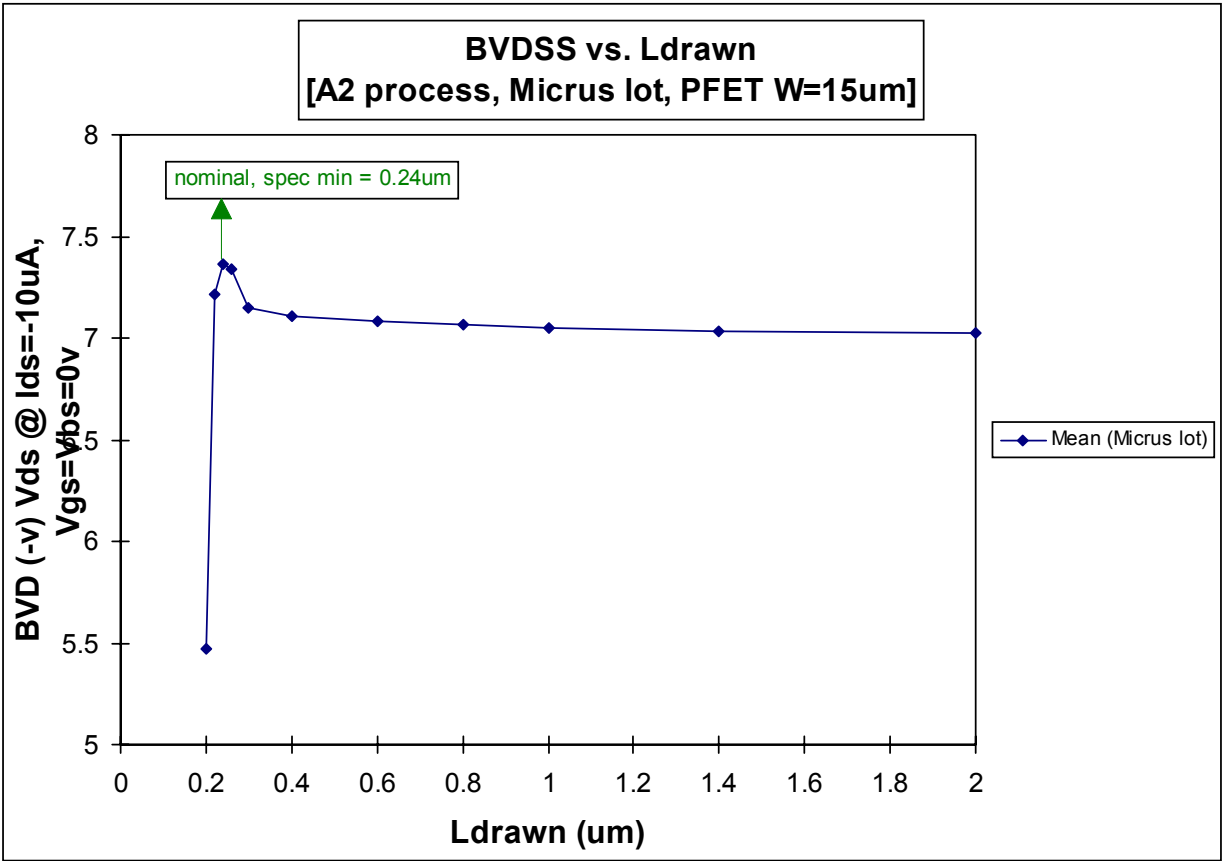


Figure 34

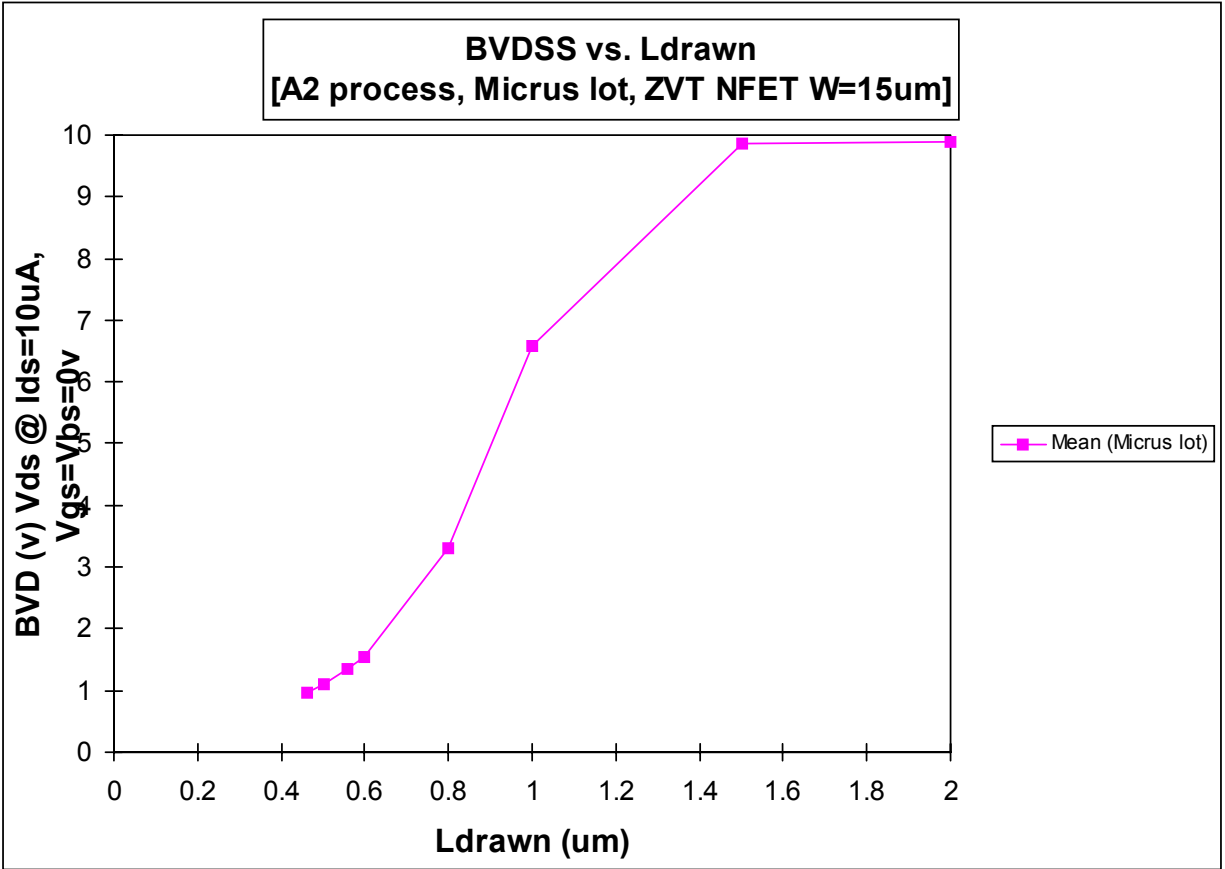


Figure 35