A2 Transistor Characterization Report (T1 Qual Lot)

Device Performance Analysis
Lot No. CYS18T02

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Silicon Technology
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- ***Overview***

This report is based on the electrical characterization data for the A2 process from a Micrus T1 qual lot. The report provides information relating to the electrical performance of transistors. A total of 3 wafers were measured on the Micrus Lot# CYS18T02 (Wafers: S6LPGUT, SWLPK2T, SNLPKAT). Nine sites were measured on each wafer (1 site at the center, 4 sites about 3cm from the edge & 4 sites about 6cm from the edge). The testing was done using the automatic prober in the Device Lab. The data from all the sites & wafers is lumped together and averaged to yield the final data.

For the graphs, each parameter is plotted against the drawn transistor length. And, only the average (mean) value of the parameter is plotted for each parameter.

Test Chip:	BATGIRL
Fab Name:	xxxxx
Process Name:	A2
Substrate Type:	P-type
Design Rule DB:	A2 (min poly = 0.24um)
Device Size Bias:	Wbias=0.0µm, Lbias(N)=0.0µm, Lbias(P)=0.0µm
Lot Number:	CYS18T02
Test Wafer ID:	S6LPGUT, SWLPK2T & SNLPKAT
Split Condition:	None
Test Sites/Wafer:	9 sites per wafer
Test Equipment:	HP4062UX Parametric Test System #2
Test Software:	*"C8 PCM Testing, rev 1.1",* May 1992, by Fred Wahl

- ***Summary of results:***

The following table summarizes the list of electrical parameters characterized in this report.

This report is based on a T1 qual lot. A similar report with an extended study will be published on the T2 qual lot.

No unusual behavior is noticed on any parameter. The nominal channel length & the poly design min are both noted on the graphs. The Delta L is calculated using the 3-point method: 2 REF devices and the DUT. The saturated Vt for the zvt device is negative. The Gamma values for the zvt device is quite low. Note that two different off-state leakage current graphs are produced. The only difference between these two is the applied gate voltage - one at 0v & the other at 0.3v.

Additionally, several ‘snapshot’ curves are included in this report. A ‘snapshot’ is a set of 4 graphs (Id-Vg-Vb (linear), Id-Vd-Vg, Id-Vg-Vb (sub-threshold) and Rout-Vd) from a single bench measurement using the BTA BSimPro Software. There are 4 ‘snapshots’ for NFET (20/0.24, 15/0.24, 1/2 & 1/0.24), 4 for PFET (15/0.24, 15/2, 1/2 , 1/0.24) & 4 for ZeroVt FET (15/0.46, 15/0.56, 15/2 & 2/0.46).Also, several temperature ‘snapshots’ are included: 20/0.24 NFET at 130^0C, 105^0C, 100^0C, 75^0C, 25^0C, 0^0C, -40^0C & -55^0C, 20/0.24 PFET at 130^0C, 105^0C, 100^0C, 75^0C, 25^0C, 0^0C, -40^0C & -55^0C and 15/0.56 ZVT NFET at 130^0C, 105^0C, 100^0C, 75^0C, 25^0C, 0^0C.

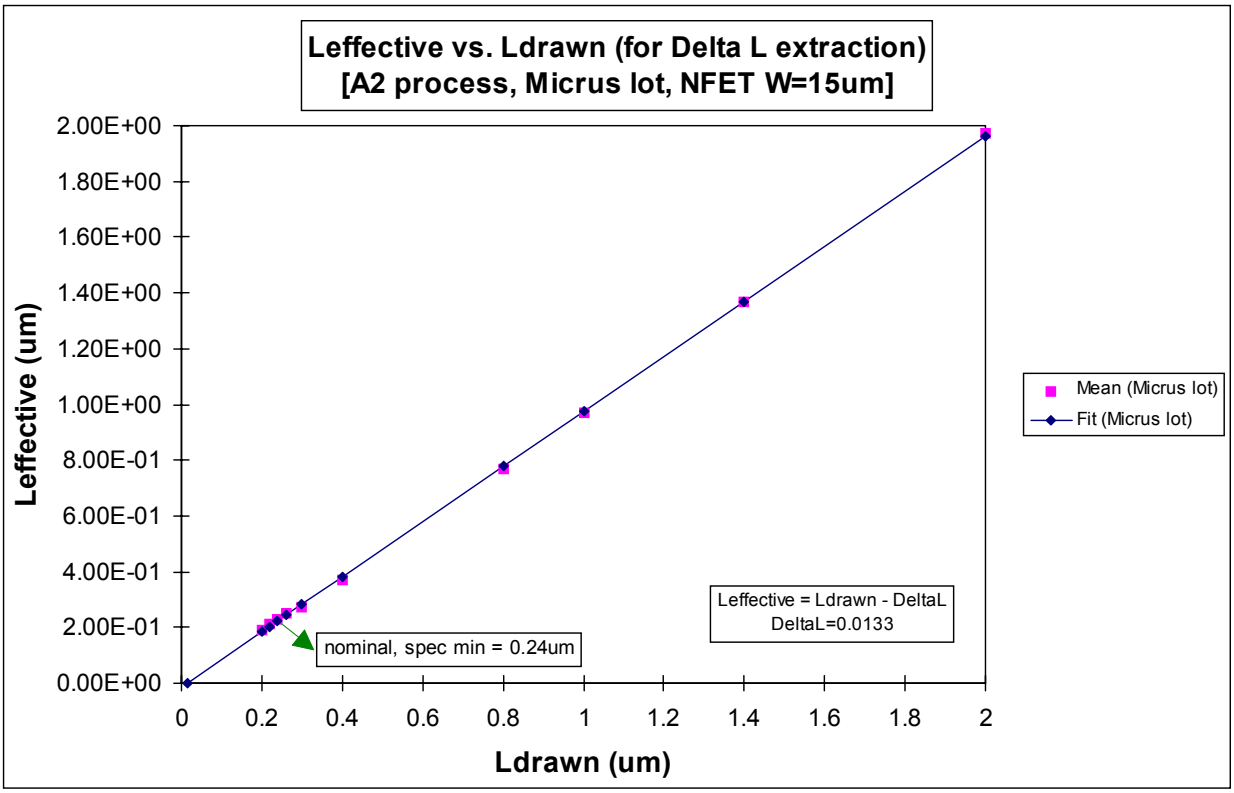

Figure 1

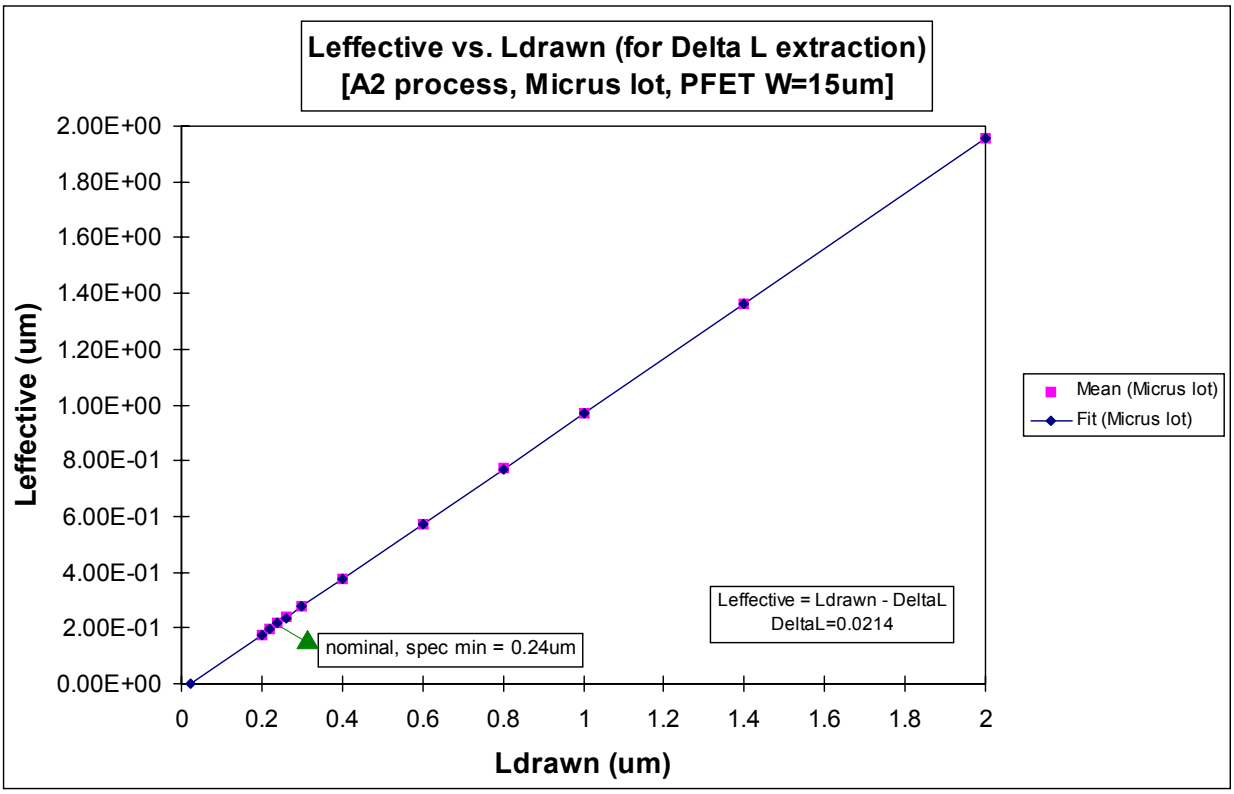

Figure 2

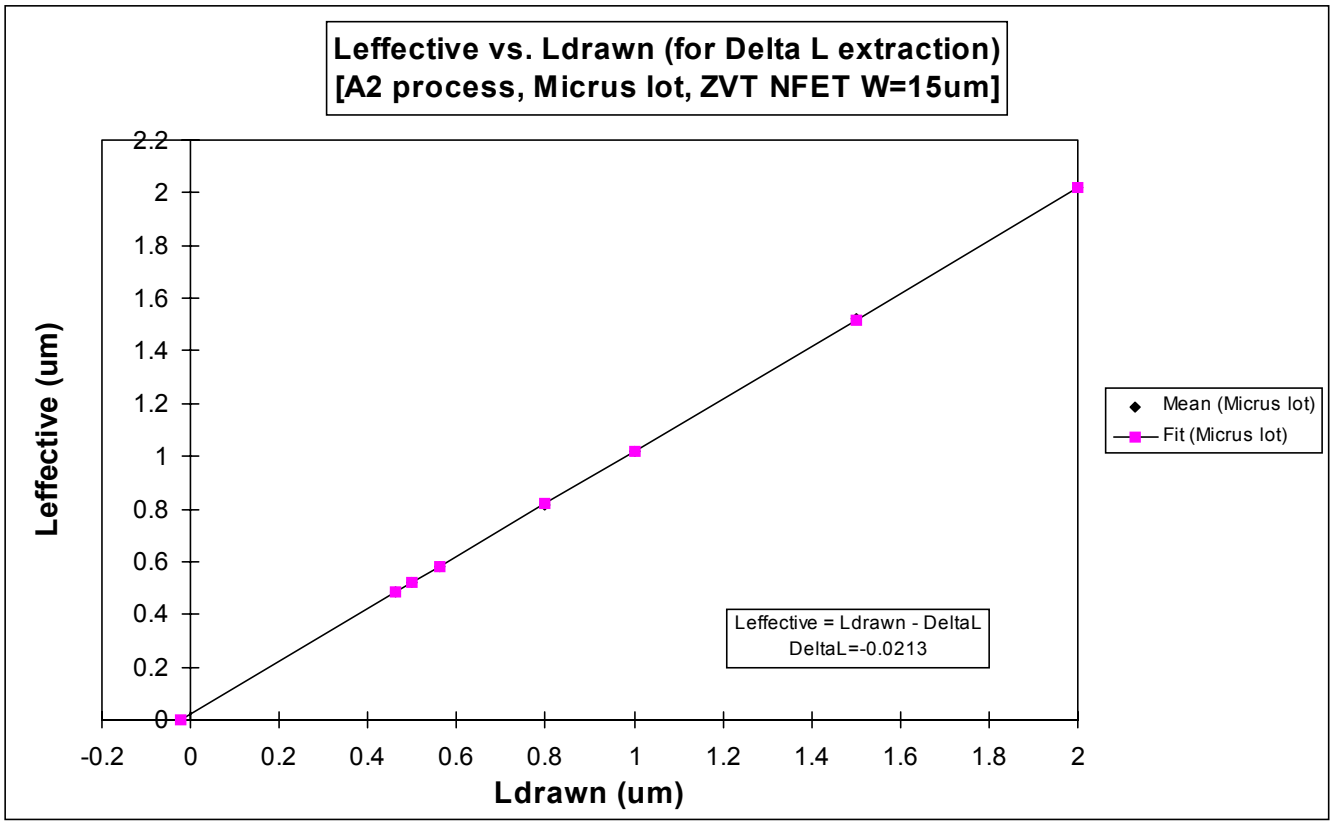
Leffective vs. Ldrawn (for Delta L extraction)
[A2 process, Micrus lot, ZVT NFET W=15um]
Leffective (um)
Ldrawn (um)
2.2
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Leffective = Ldrawn - DeltaL
DeltaL=-0.0213
Mean (Micrus lot)
Fit (Micrus lot)

Figure 3

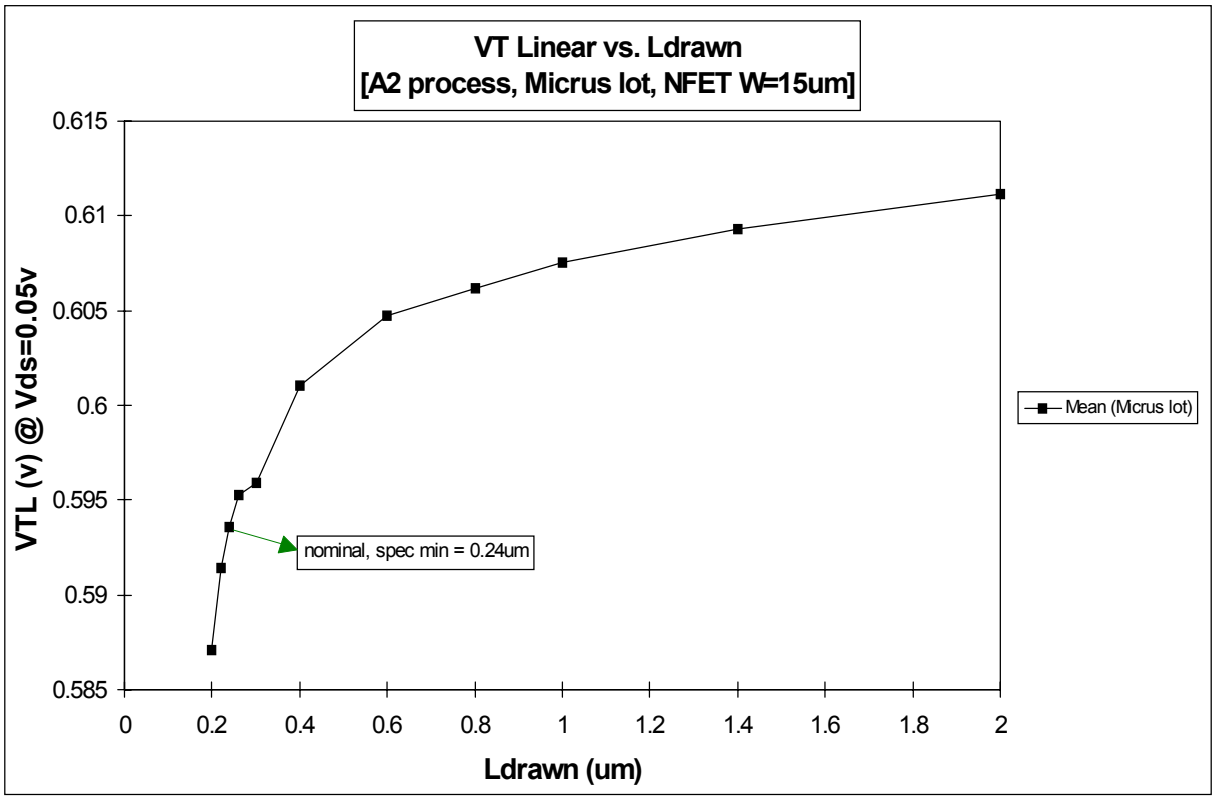

Figure 4

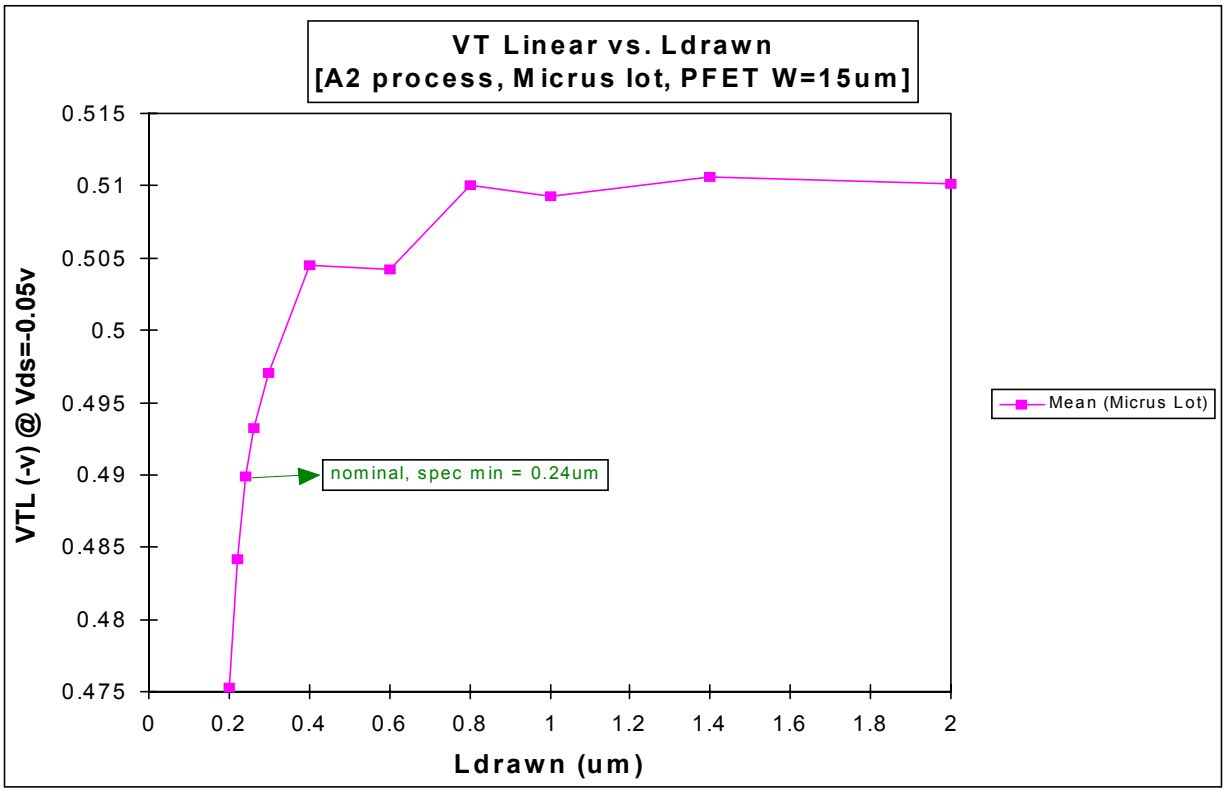

Figure 5

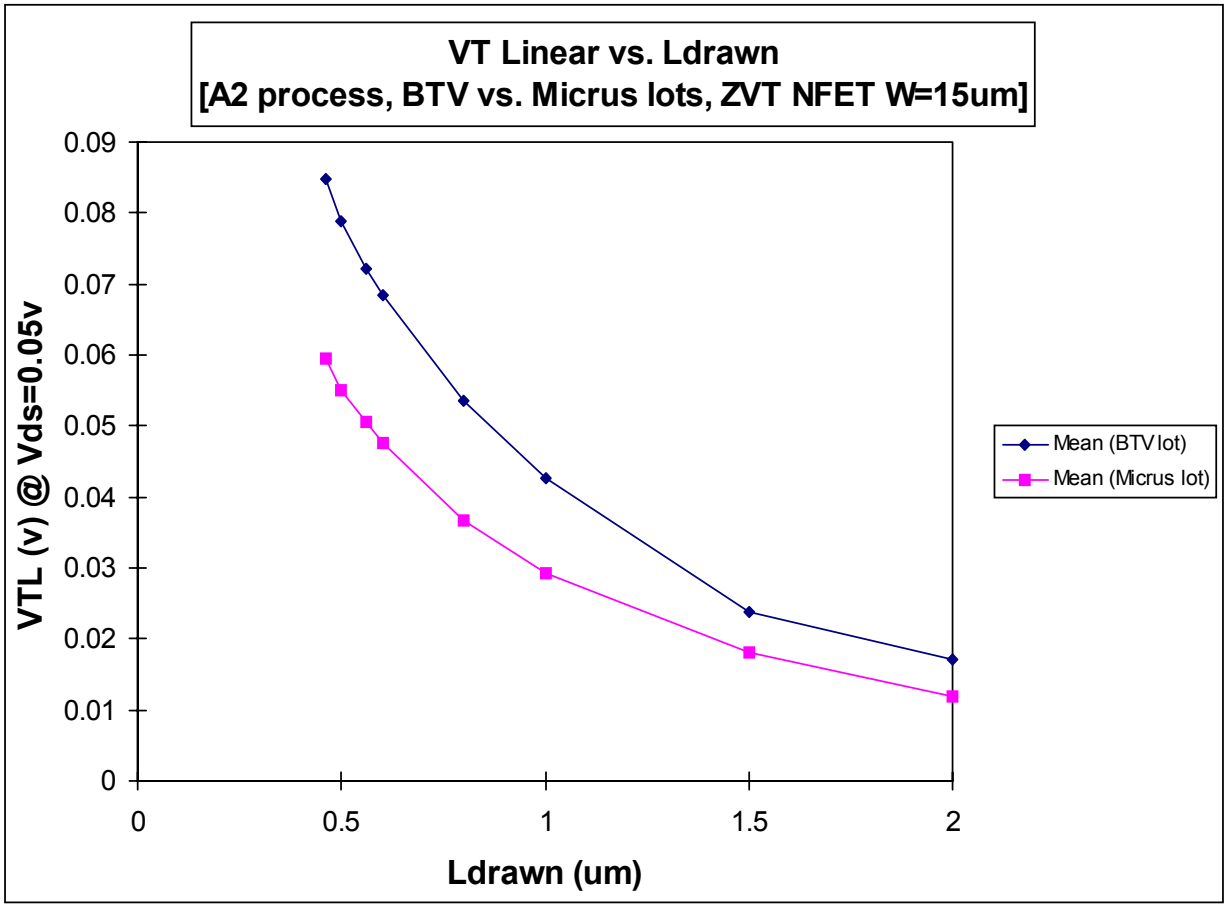
VT Linear vs. Ldrawn
[A2 process, BTV vs. Micrus lots, ZVT NFET W=15um]
VTL (v) @ Vds=0.05v
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
0.5
1
1.5
2
Ldrawn (um)
Mean (BTV lot)
Mean (Micrus lot)

Figure 6

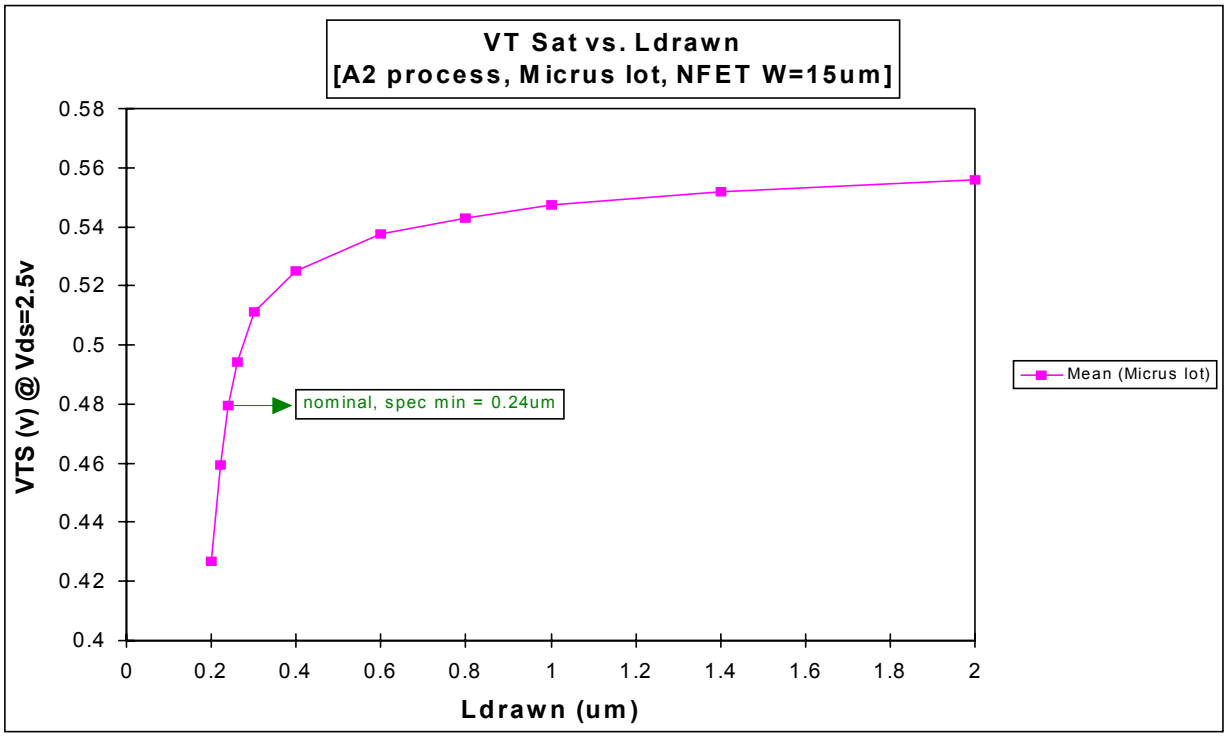

Figure 7

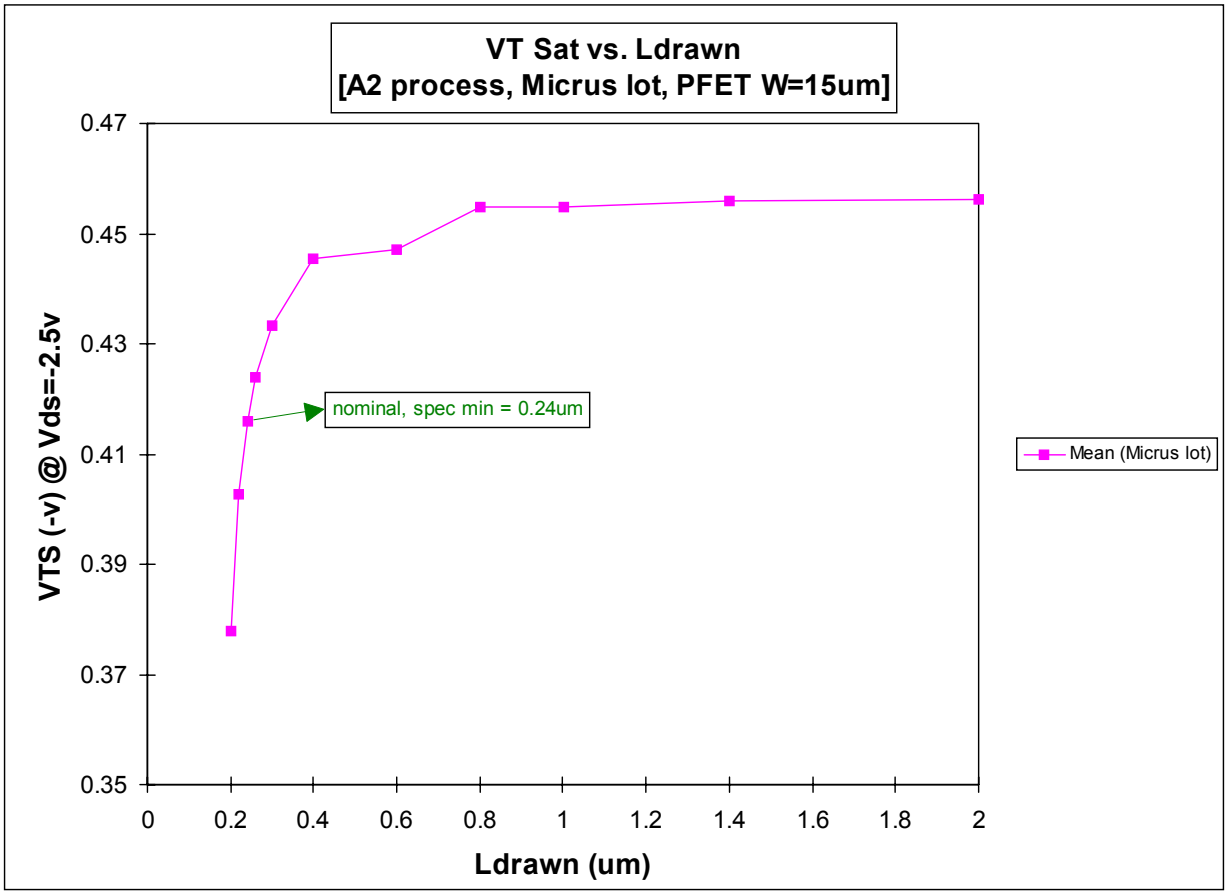

Figure 8

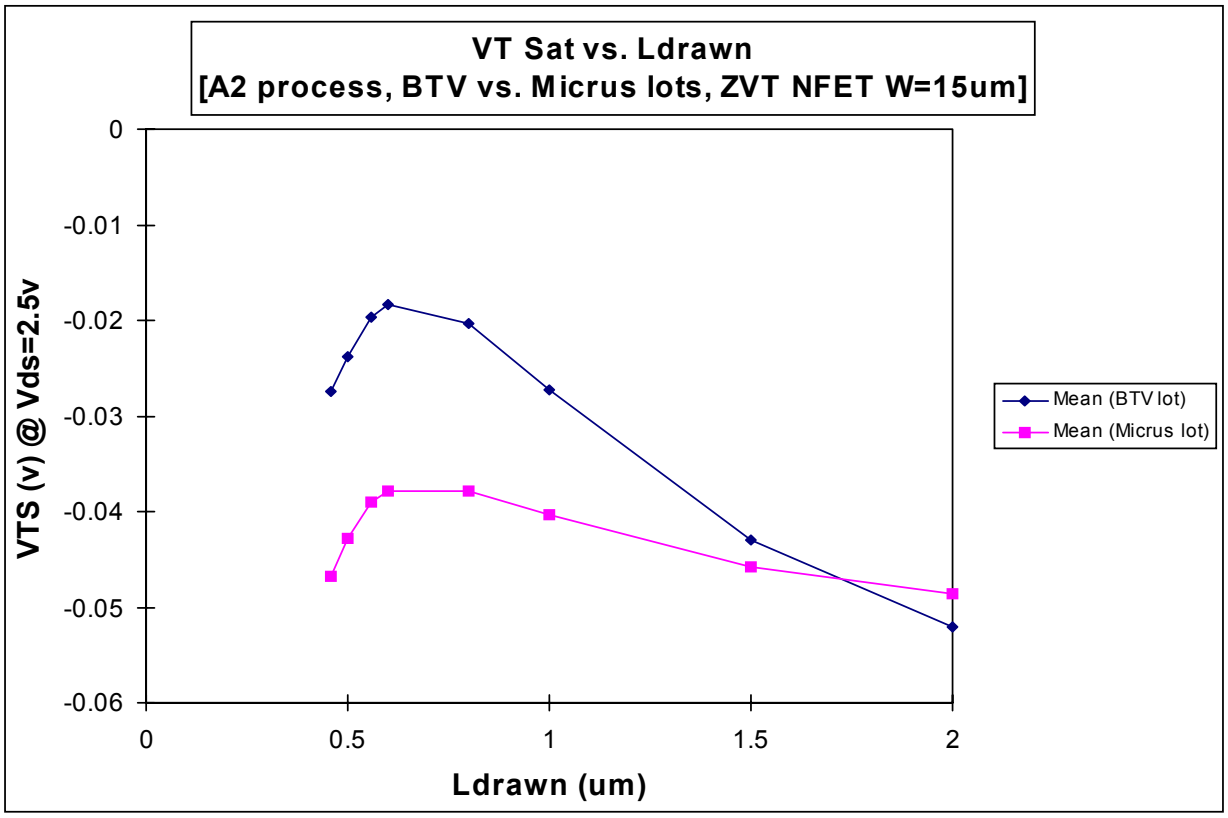
VT Sat vs. Ldrawn
[A2 process, BTV vs. Micrus lots, ZVT NFET W=15um]
VTS (v) @ Vds=2.5v
0
-0.01
-0.02
-0.03
-0.04
-0.05
-0.06
0
0.5
1
1.5
2
Ldrawn (um)
Mean (BTV lot)
Mean (Micrus lot)

Figure 9

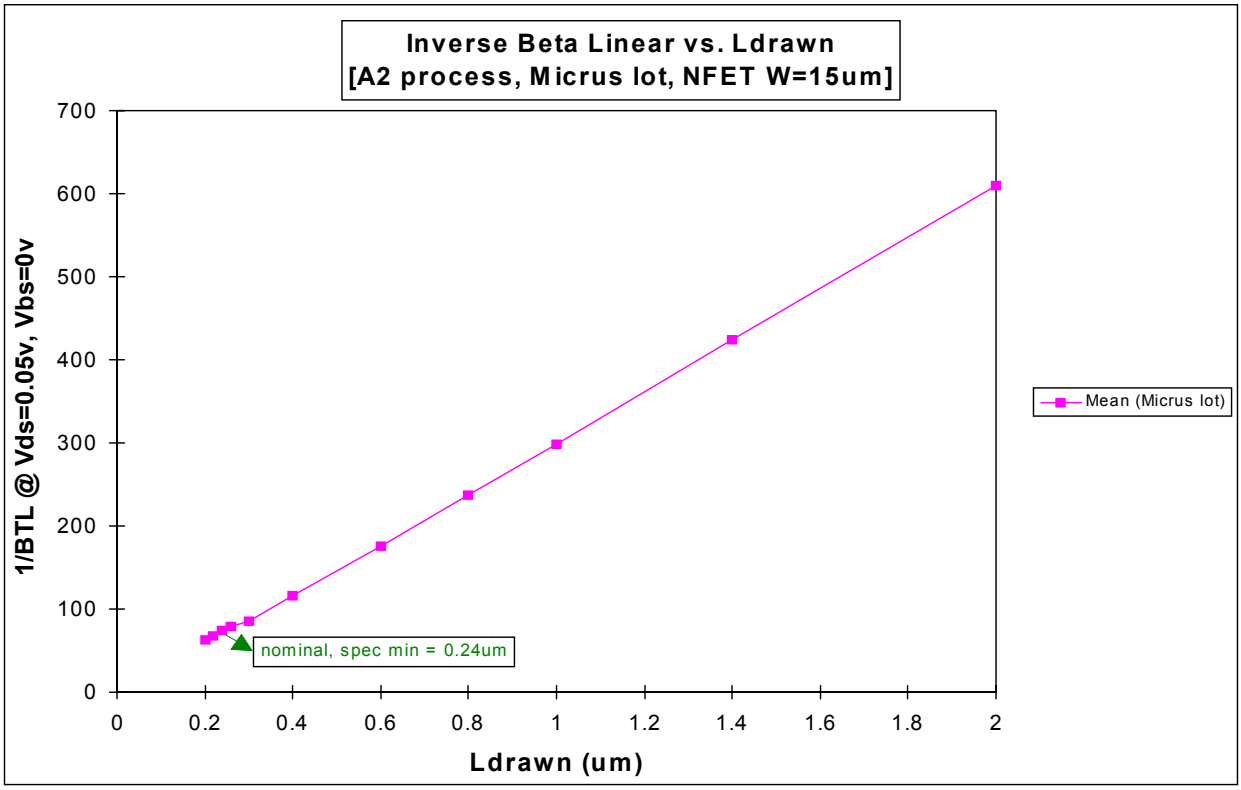

Figure 10

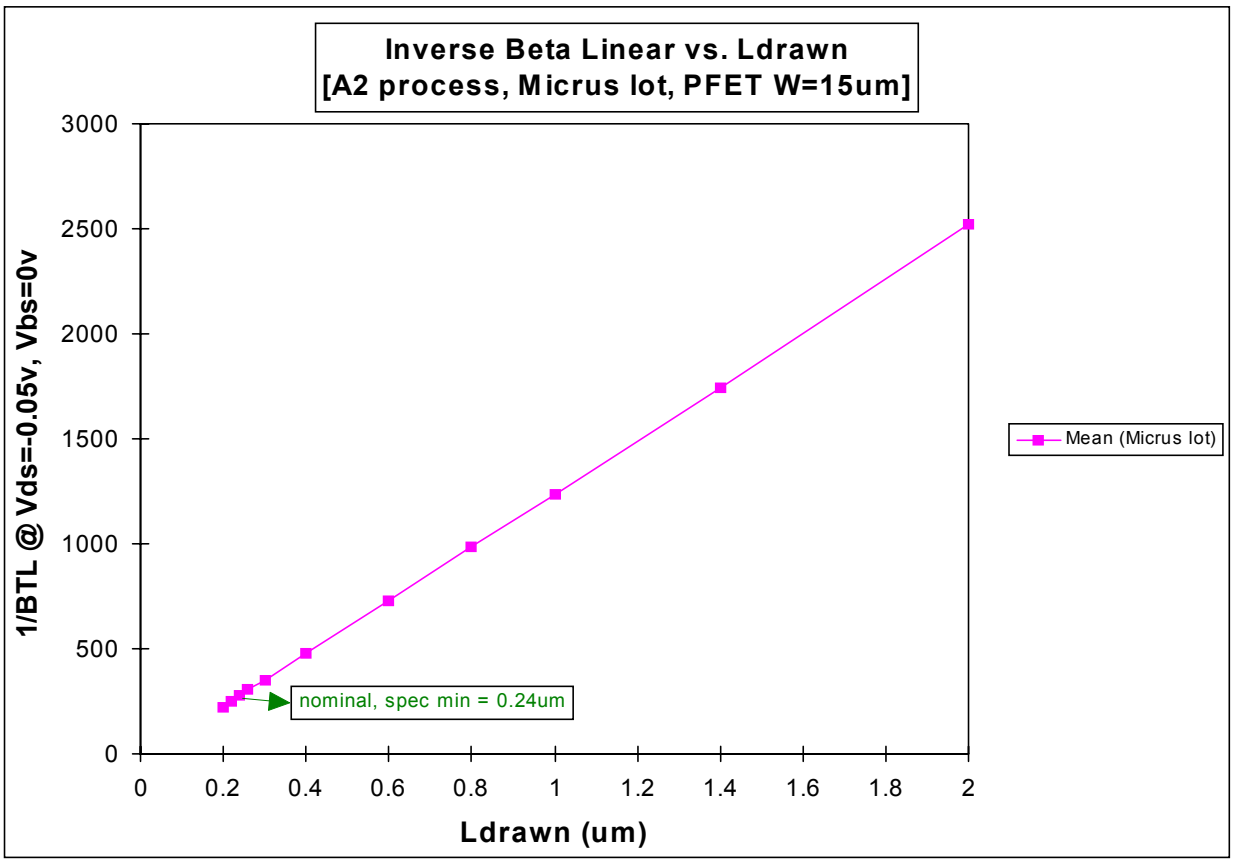

Figure 11

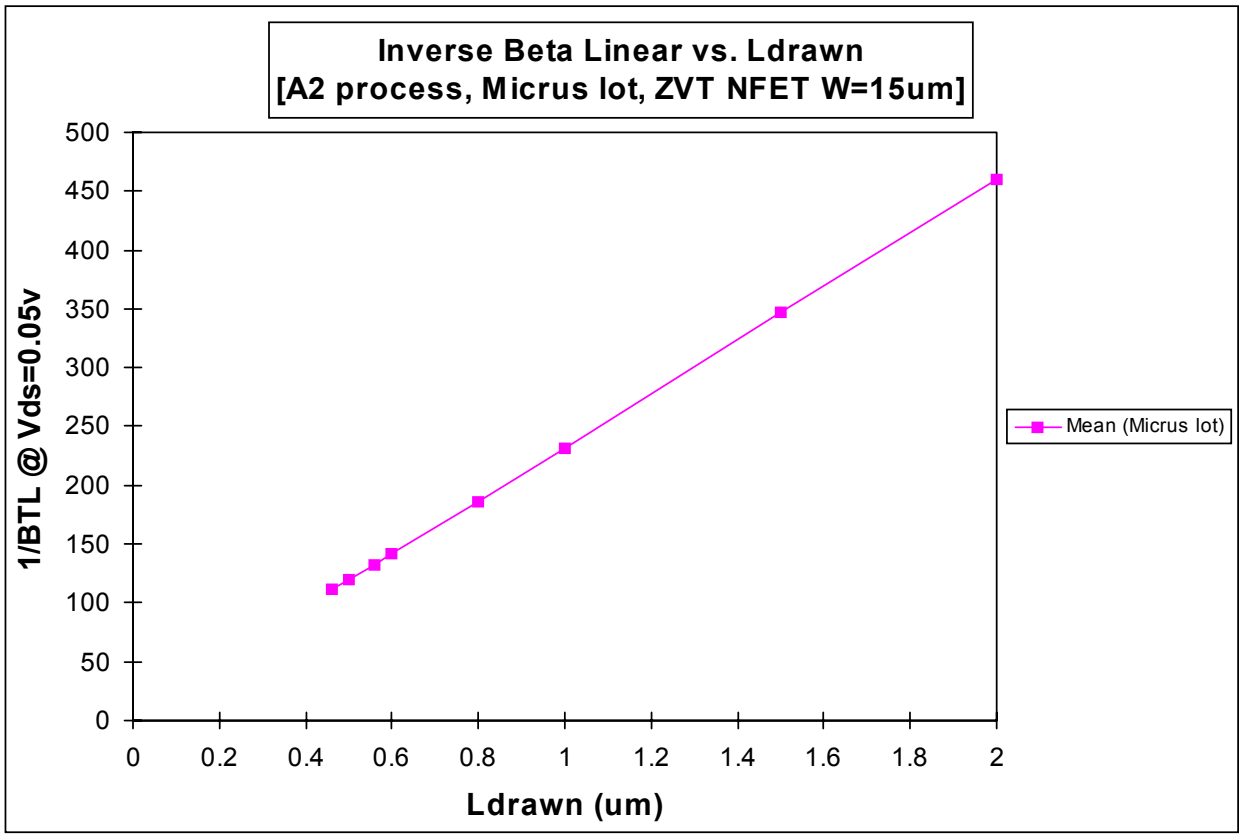
Inverse Beta Linear vs. Ldrawn
[A2 process, Micrus lot, ZVT NFET W=15um]
1/BTL @ Vds=0.05v
500
450
400
350
300
250
200
150
100
50
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Ldrawn (um)
Mean (Micrus lot)

Figure 12

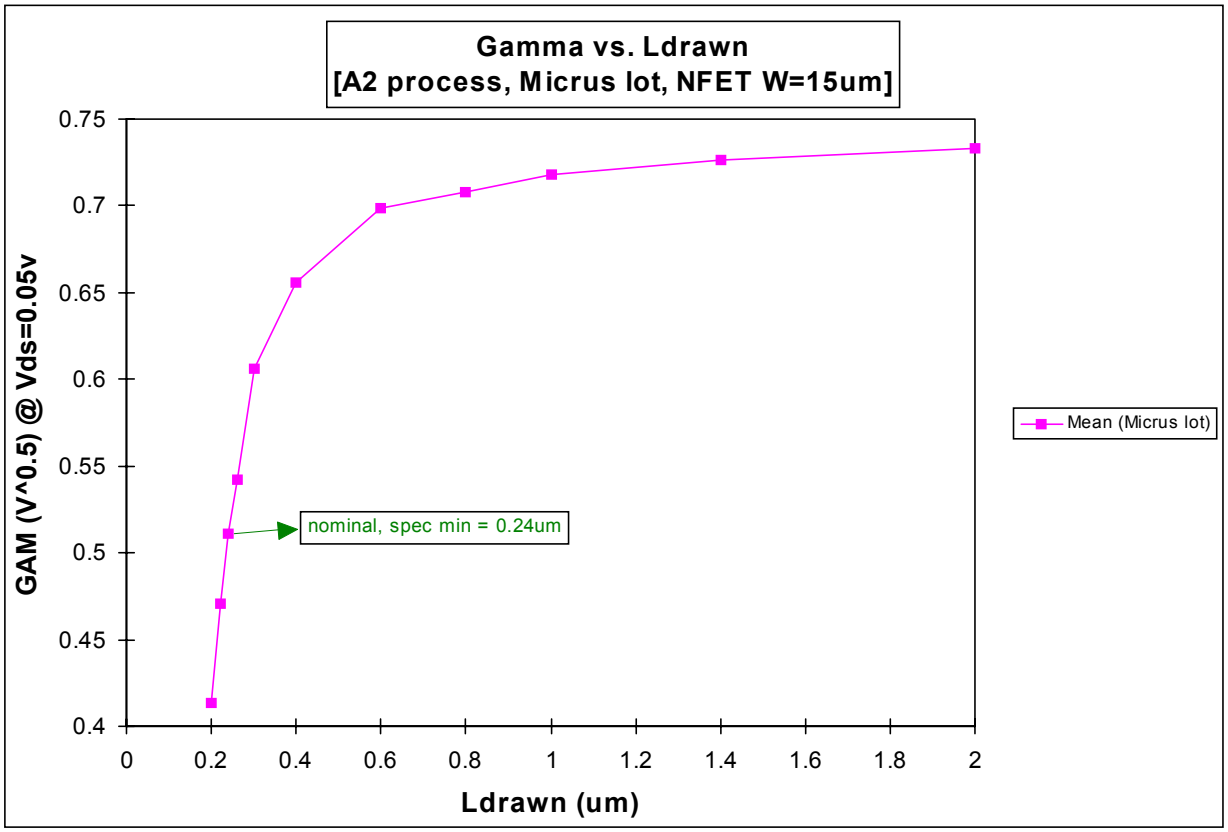

Figure 13

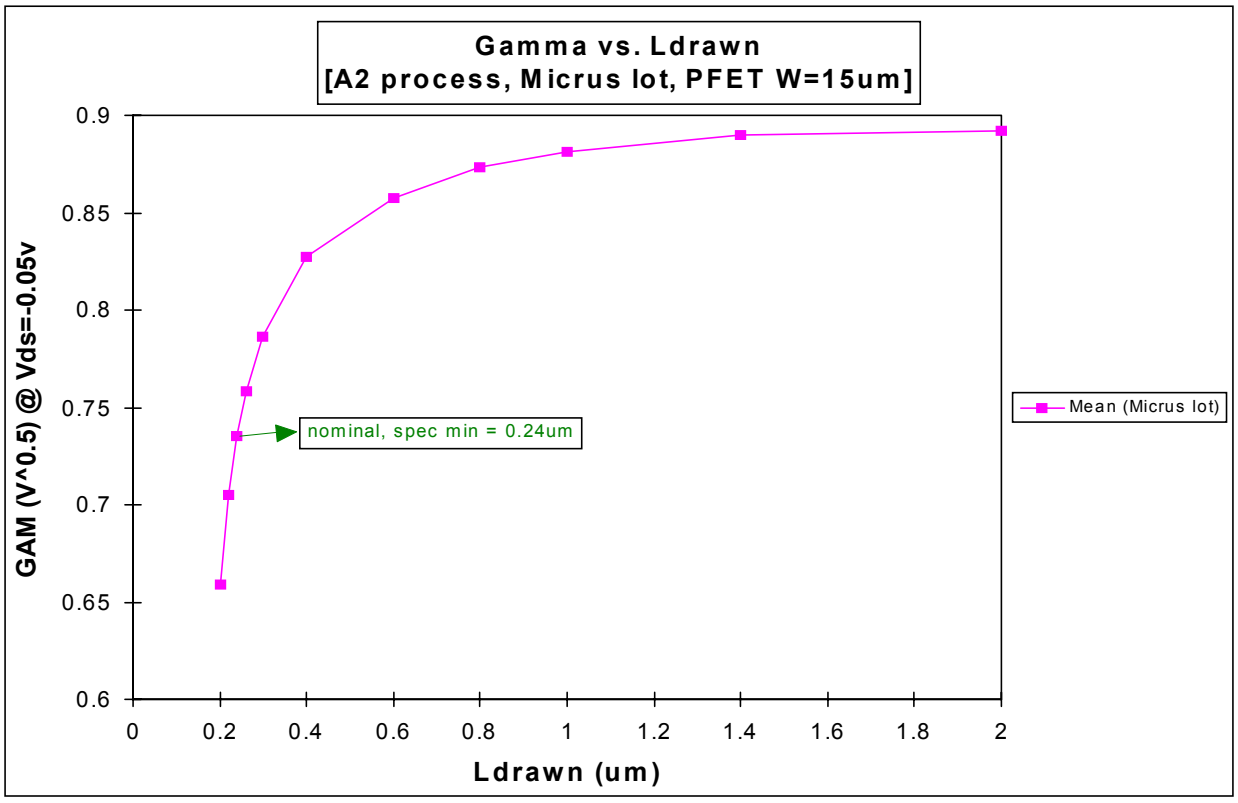

Figure 14

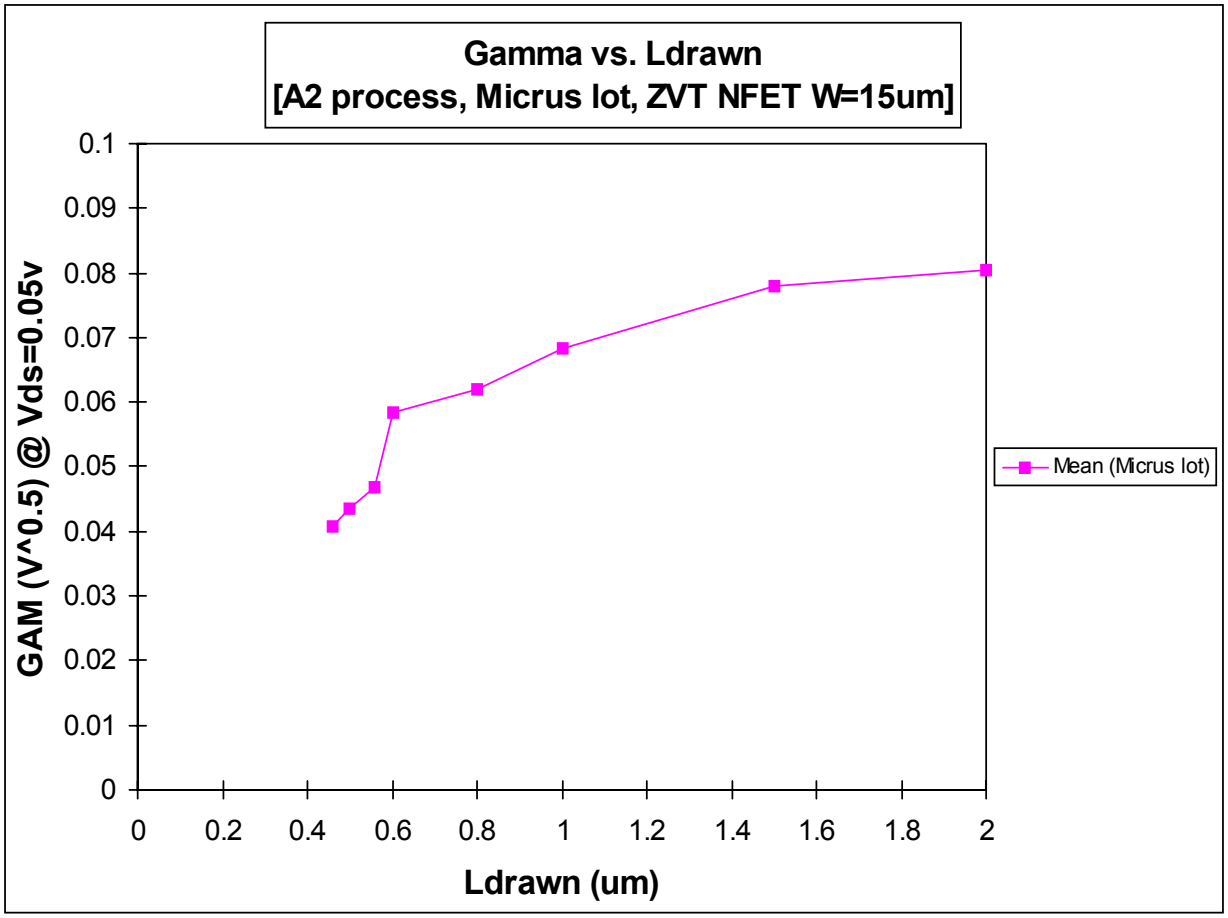
Gamma vs. Ldrawn
[A2 process, Micrus lot, ZVT NFET W=15um]
GAM (V^0.5) @ Vds=0.05v
0.1
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Ldrawn (um)
Mean (Micrus lot)

Figure 15

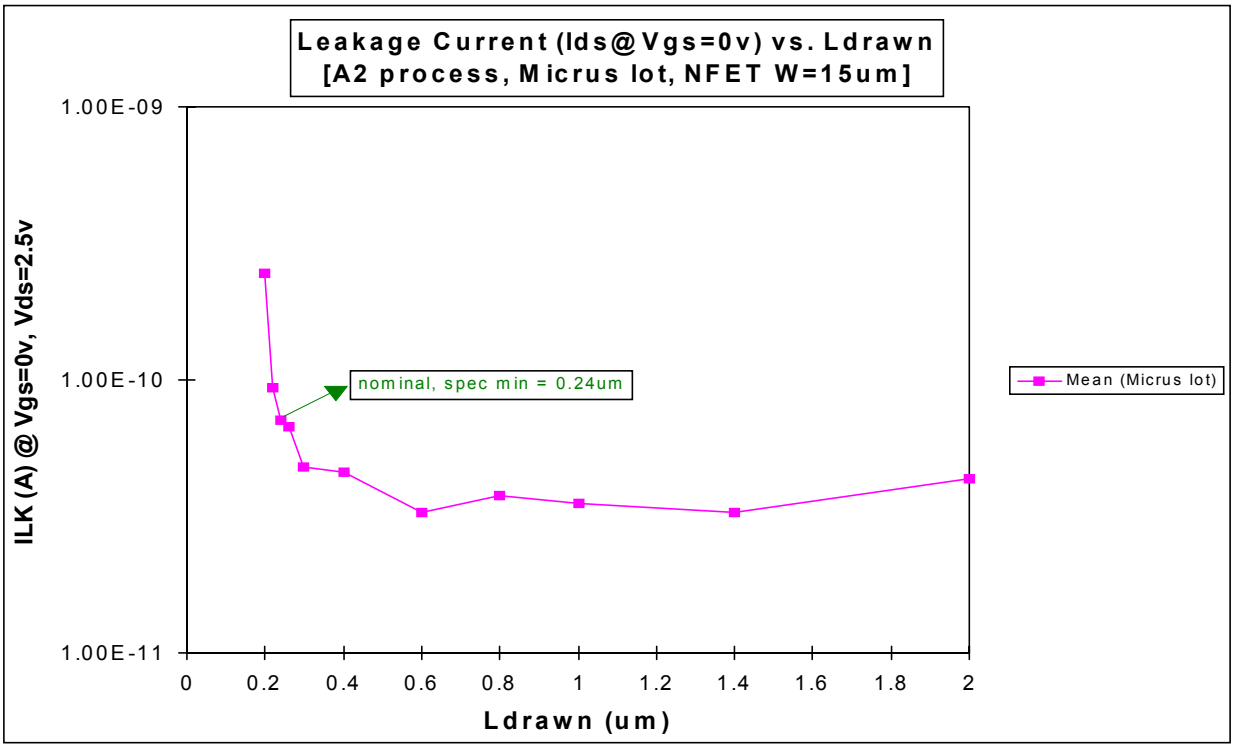

Figure 16

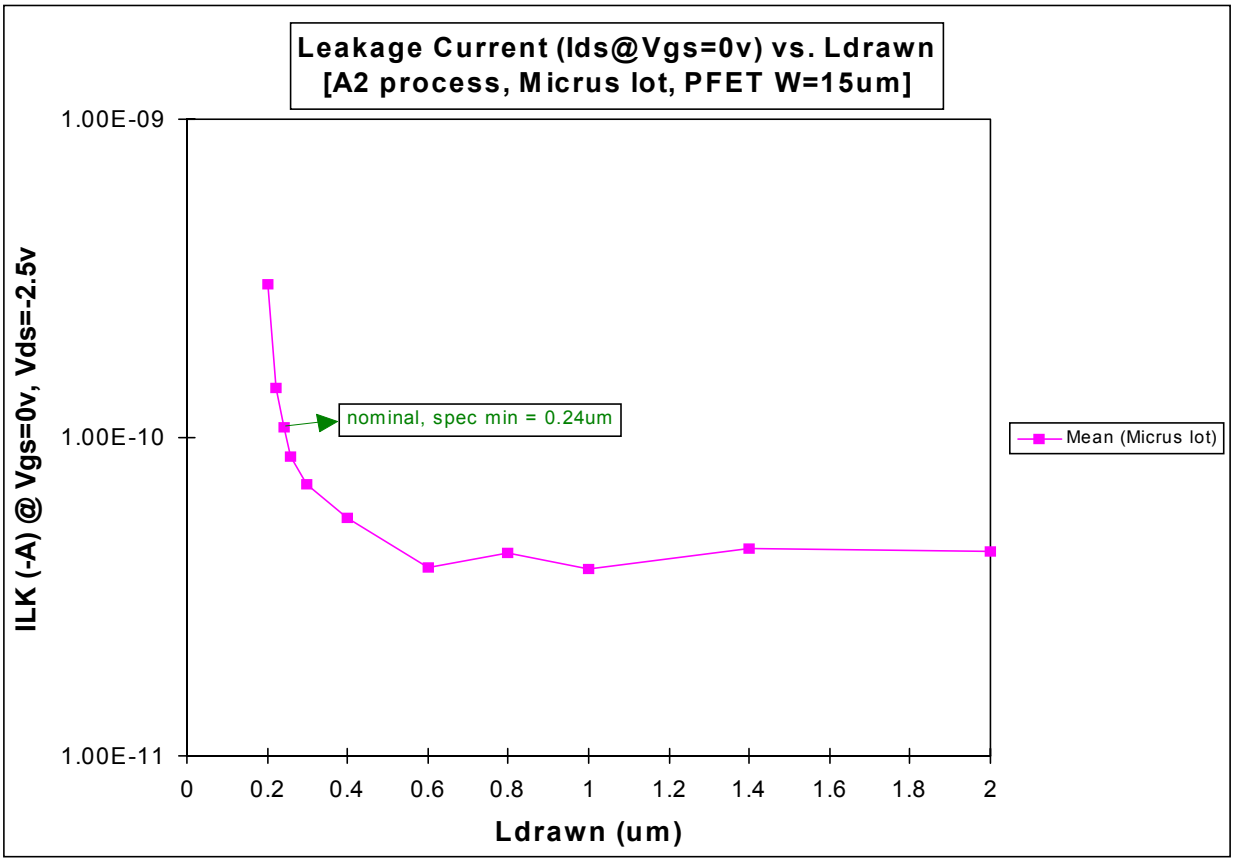

Figure 17

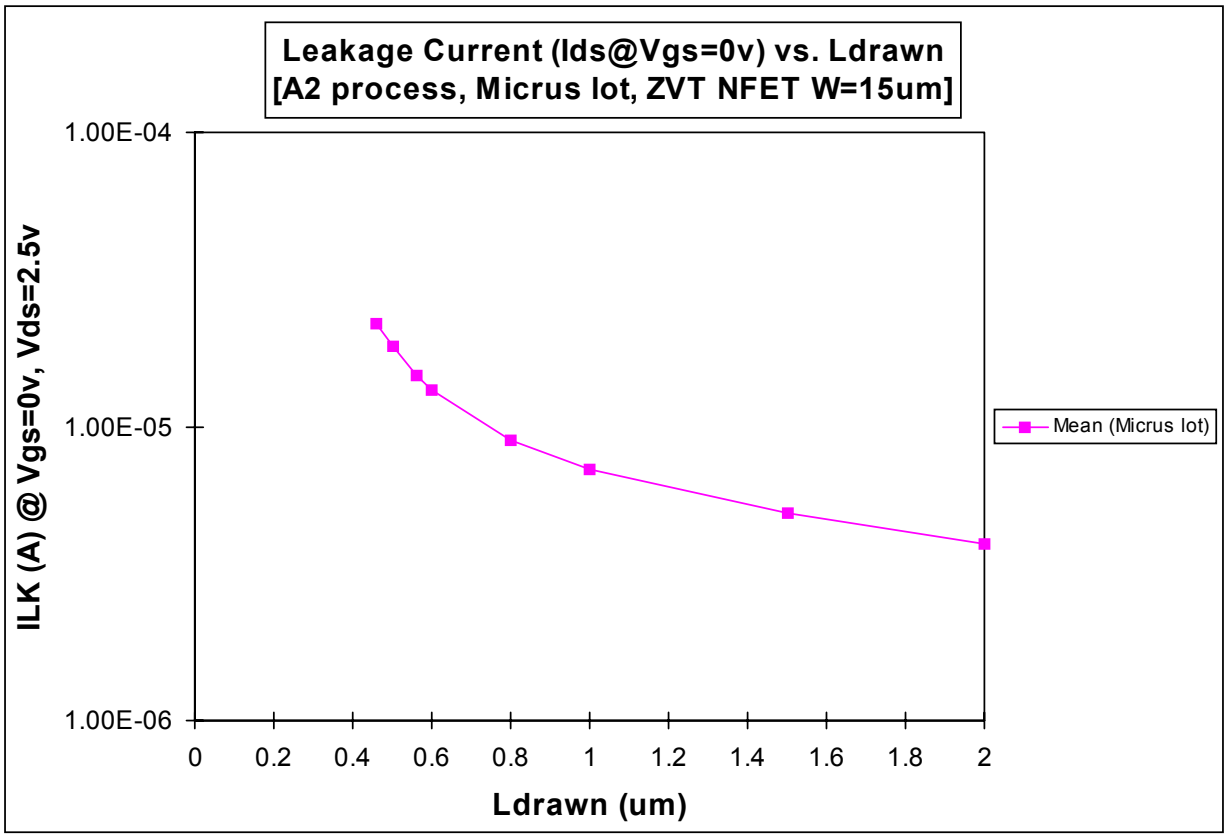
Leakage Current (Ids@Vgs=0v) vs. Ldrawn
[A2 process, Micrus lot, ZVT NFET W=15um]
1.00E-04
1.00E-05
1.00E-06
ILK (A) @ Vgs=0v, Vds=2.5v
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Ldrawn (um)
Mean (Micrus lot)

Figure 18

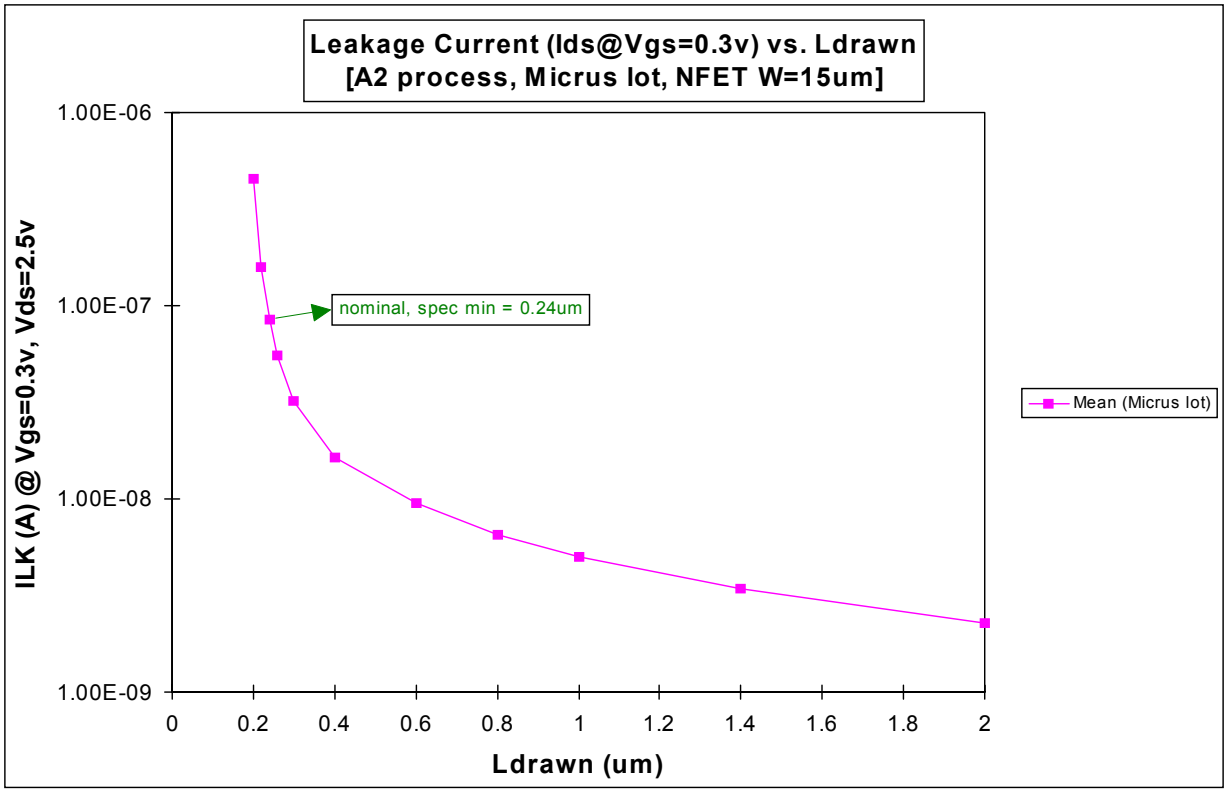

Figure 19

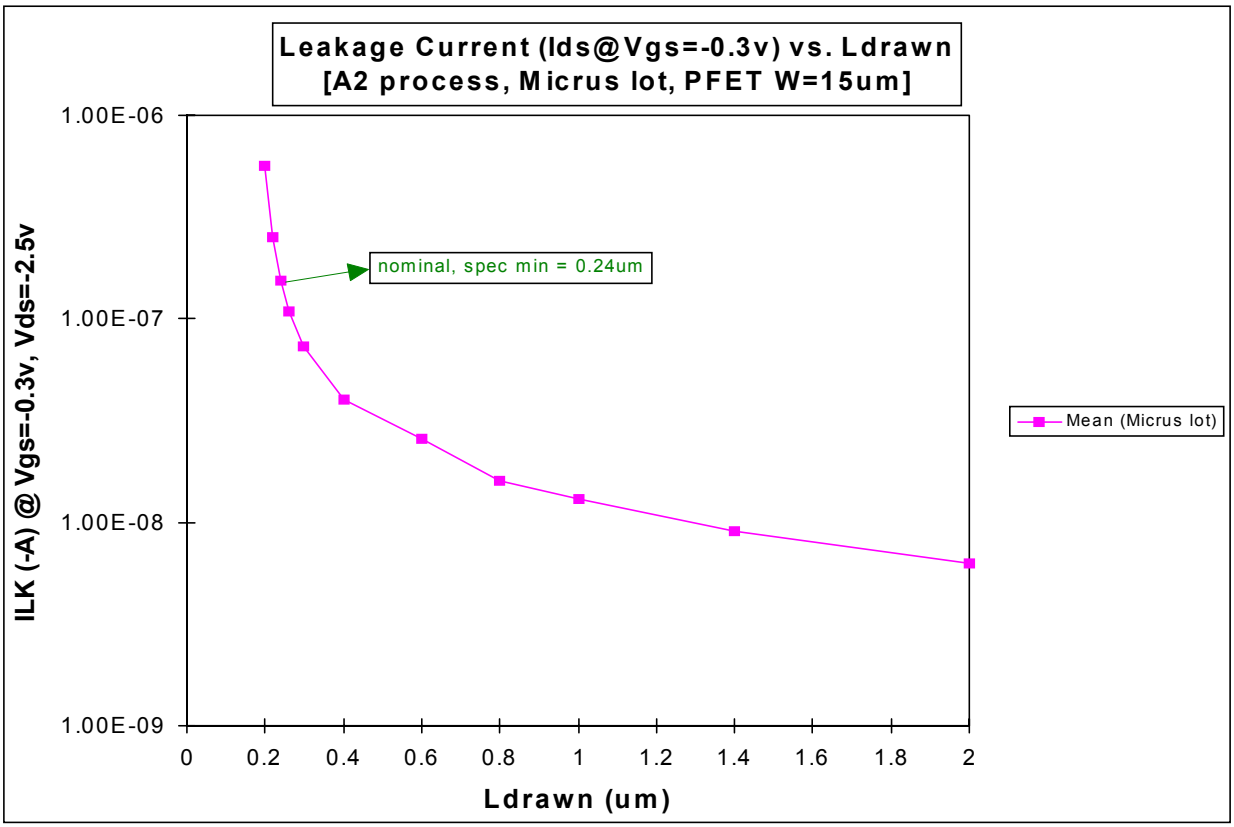

Figure 20

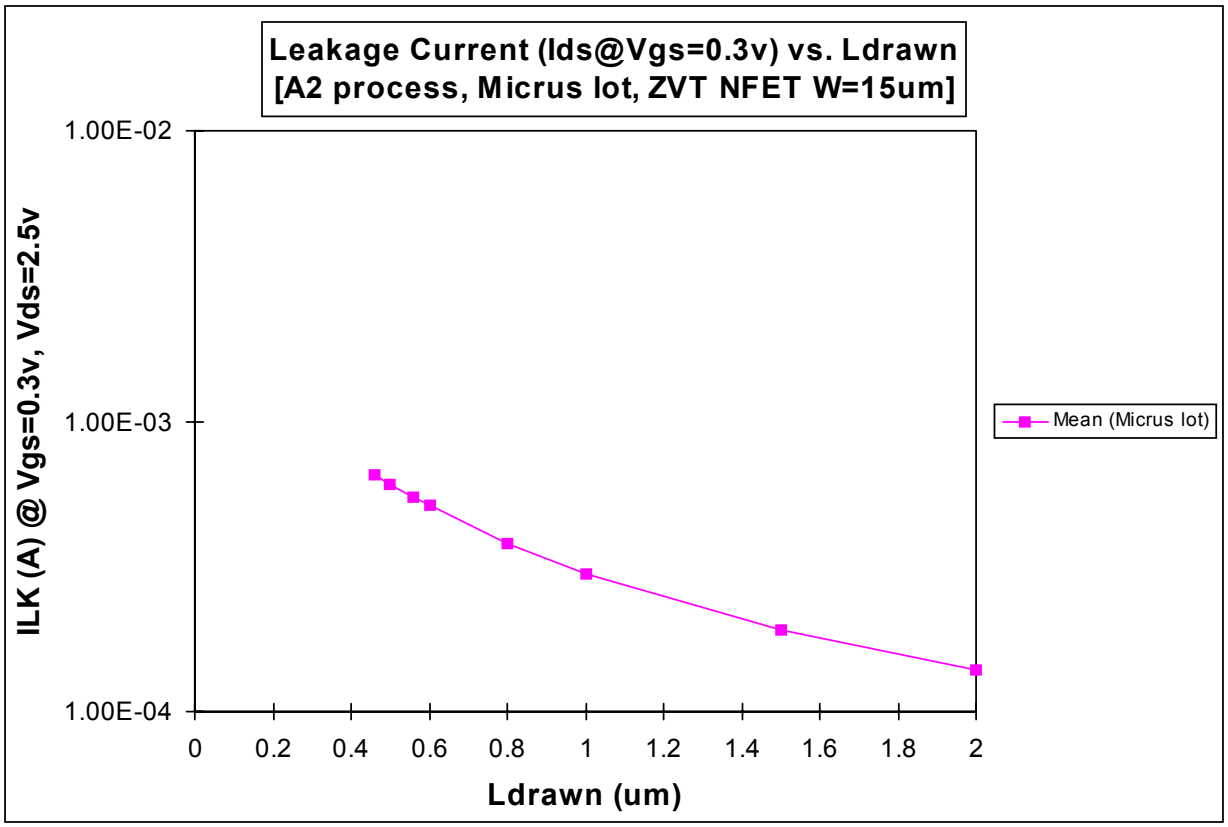
Leakage Current (Ids@Vgs=0.3v) vs. Ldrawn
[A2 process, Micrus lot, ZVT NFET W=15um]
ILK (A) @ Vgs=0.3v, Vds=2.5v
1.00E-02
1.00E-03
1.00E-04
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Ldrawn (um)
Mean (Micrus lot)

Figure 21

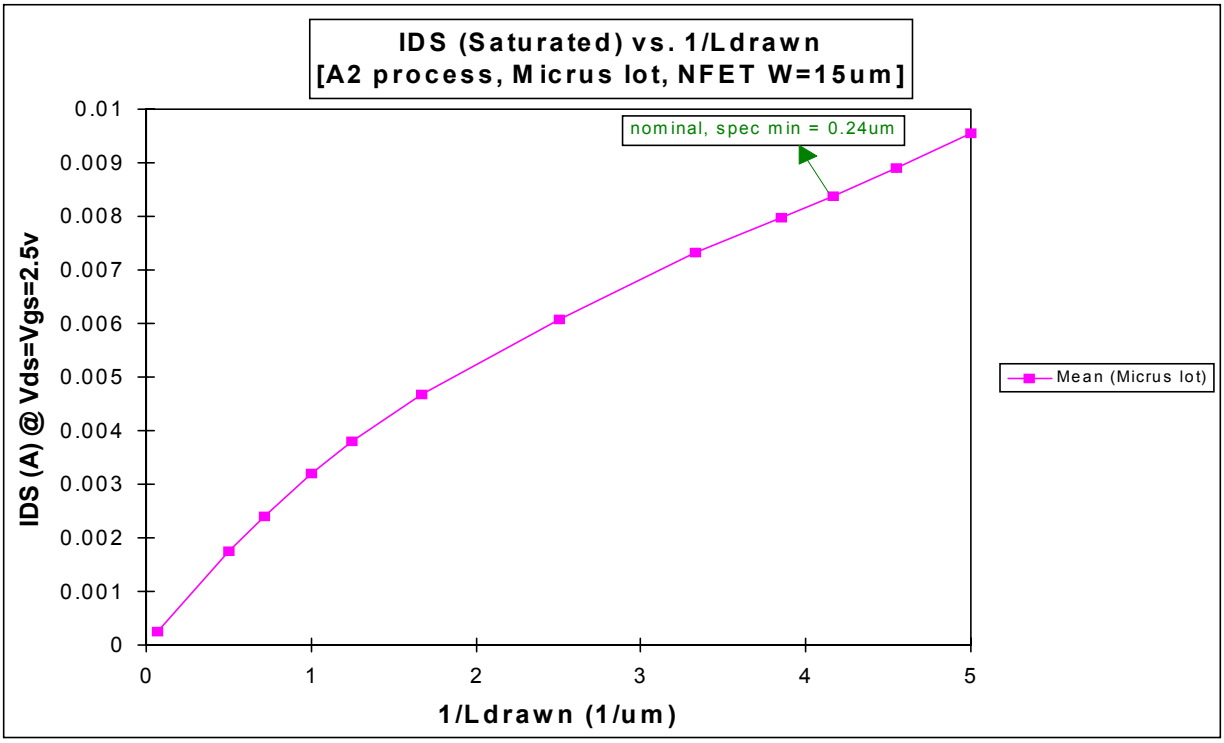

Figure 22

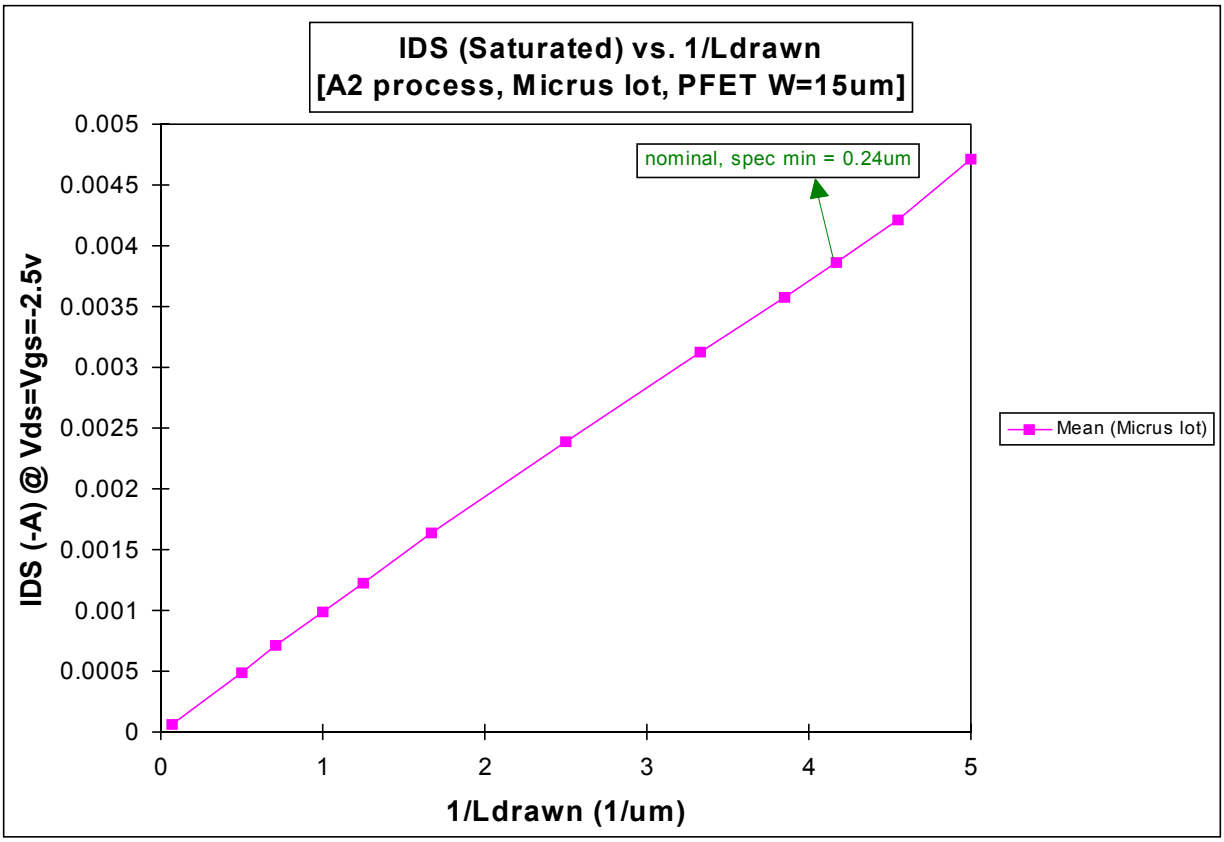

Figure 23

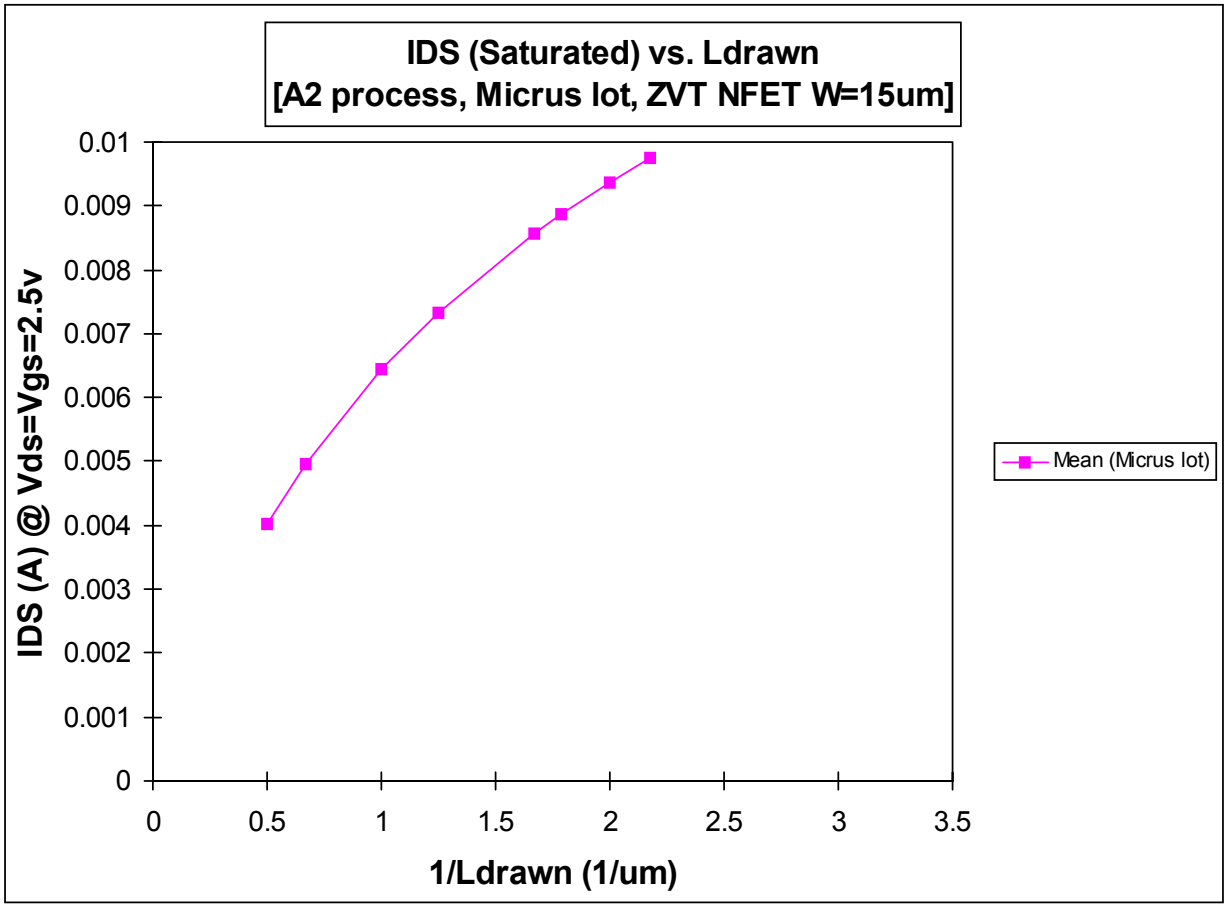
IDS (Saturated) vs. Ldrawn
[A2 process, Micrus lot, ZVT NFET W=15um]
IDS (A) @ Vds=Vgs=2.5v
0.01
0.009
0.008
0.007
0.006
0.005
0.004
0.003
0.002
0.001
0
0
0.5
1
1.5
2
2.5
3
3.5
1/Ldrawn (1/um)
Mean (Micrus lot)

Figure 24

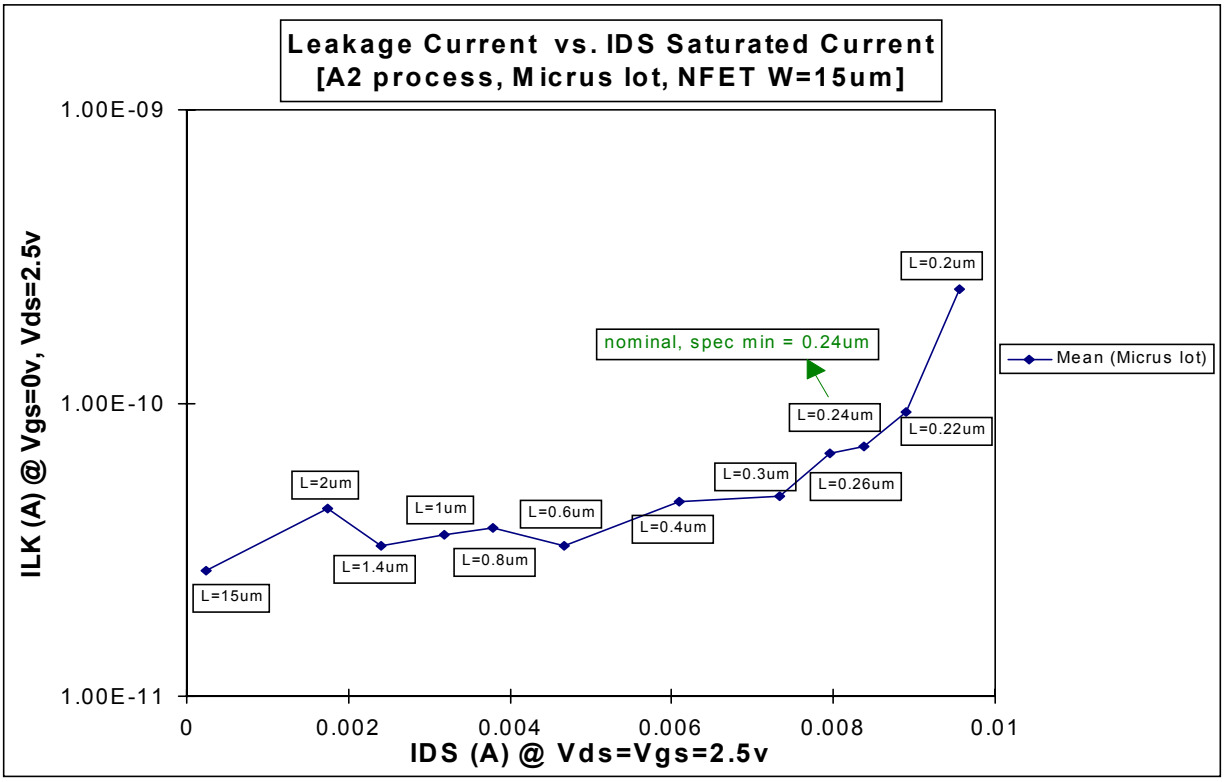

Figure 25

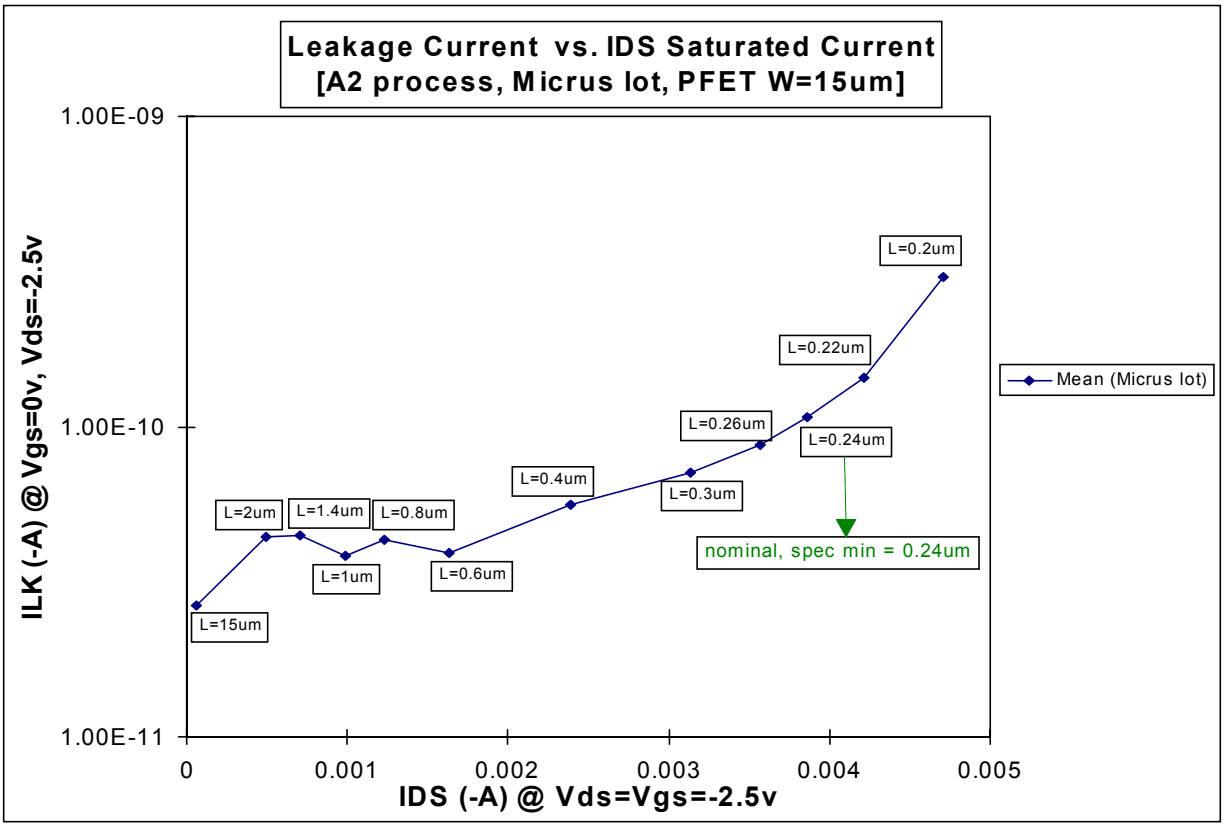

Figure 26

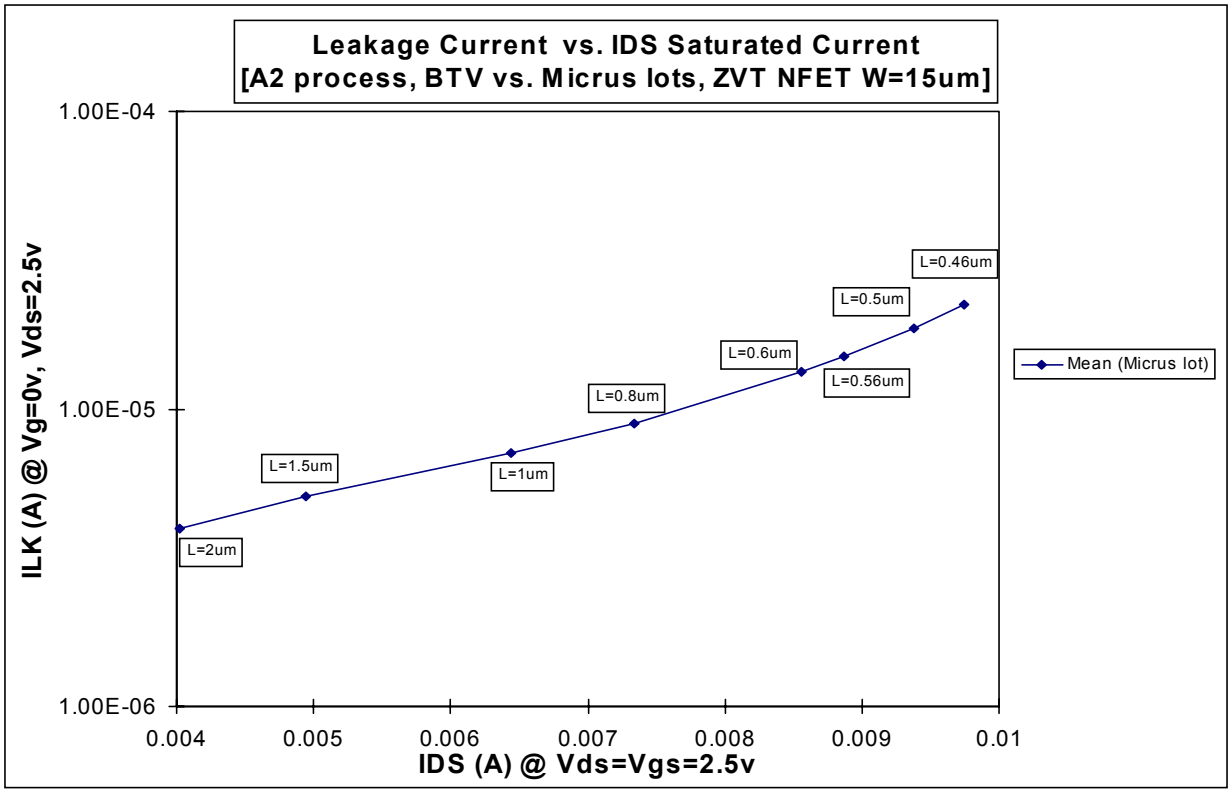
Leakage Current vs. IDS Saturated Current
[A2 process, BTV vs. Micrus lots, ZVT NFET W=15um]
1.00E-04
1.00E-05
1.00E-06
ILK (A) @ Vg=0v, Vds=2.5v
0.004
0.005
0.006
0.007
0.008
0.009
0.01
IDS (A) @ Vds=Vgs=2.5v
L=2um
L=1.5um
L=1um
L=0.8um
L=0.6um
L=0.56um
L=0.5um
L=0.46um
Mean (Micrus lot)

Figure 27

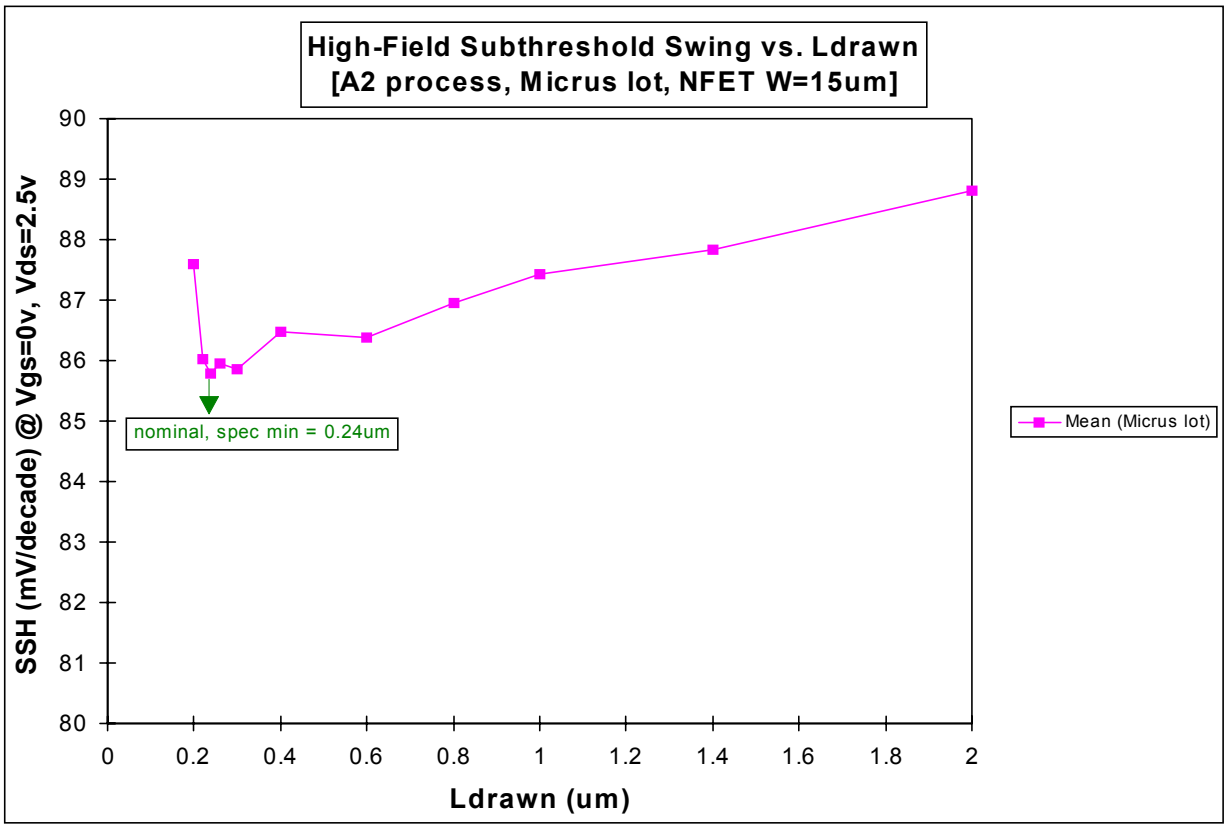
High-Field Subthreshold Swing vs. Ldrawn
[A2 process, Micrus lot, NFET W=15um]
90
89
88
87
86
85
84
83
82
81
80
SSH (mV/decade) @ Vgs=0v, Vds=2.5v
nominal, spec min = 0.24um
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Ldrawn (um)
Mean (Micrus lot)

Figure 28

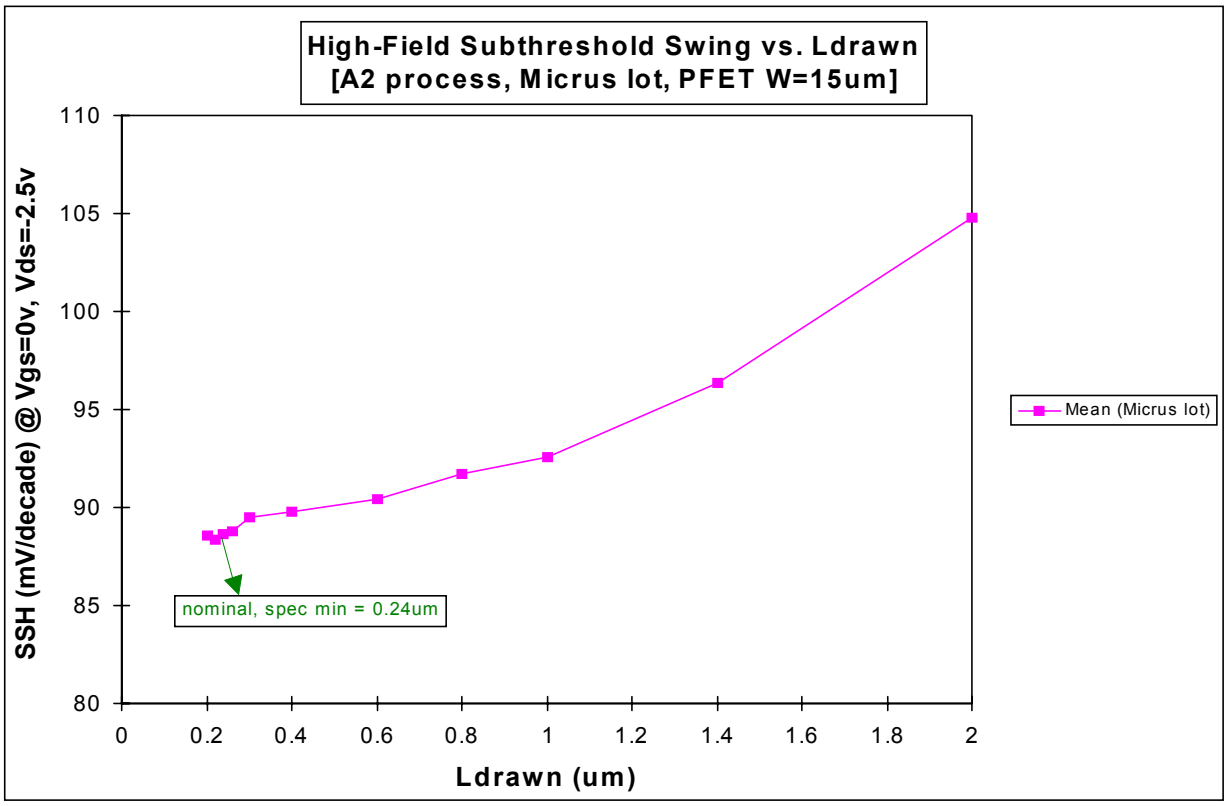

Figure 29

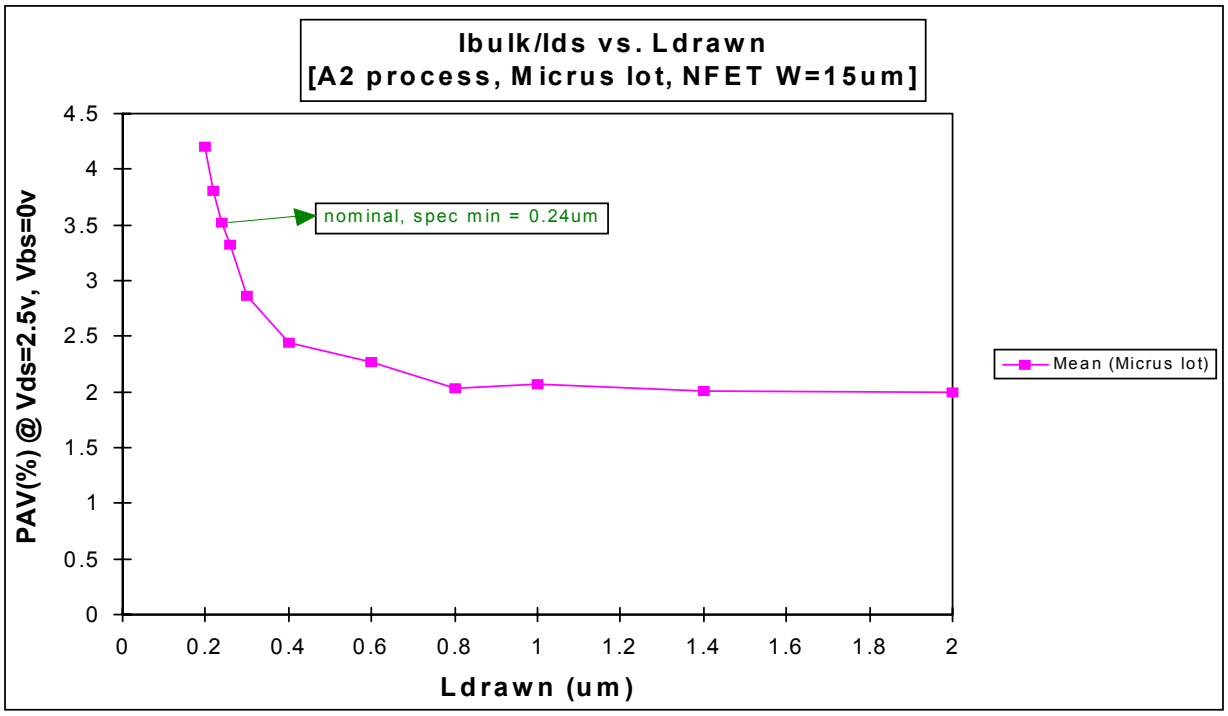

Figure 30

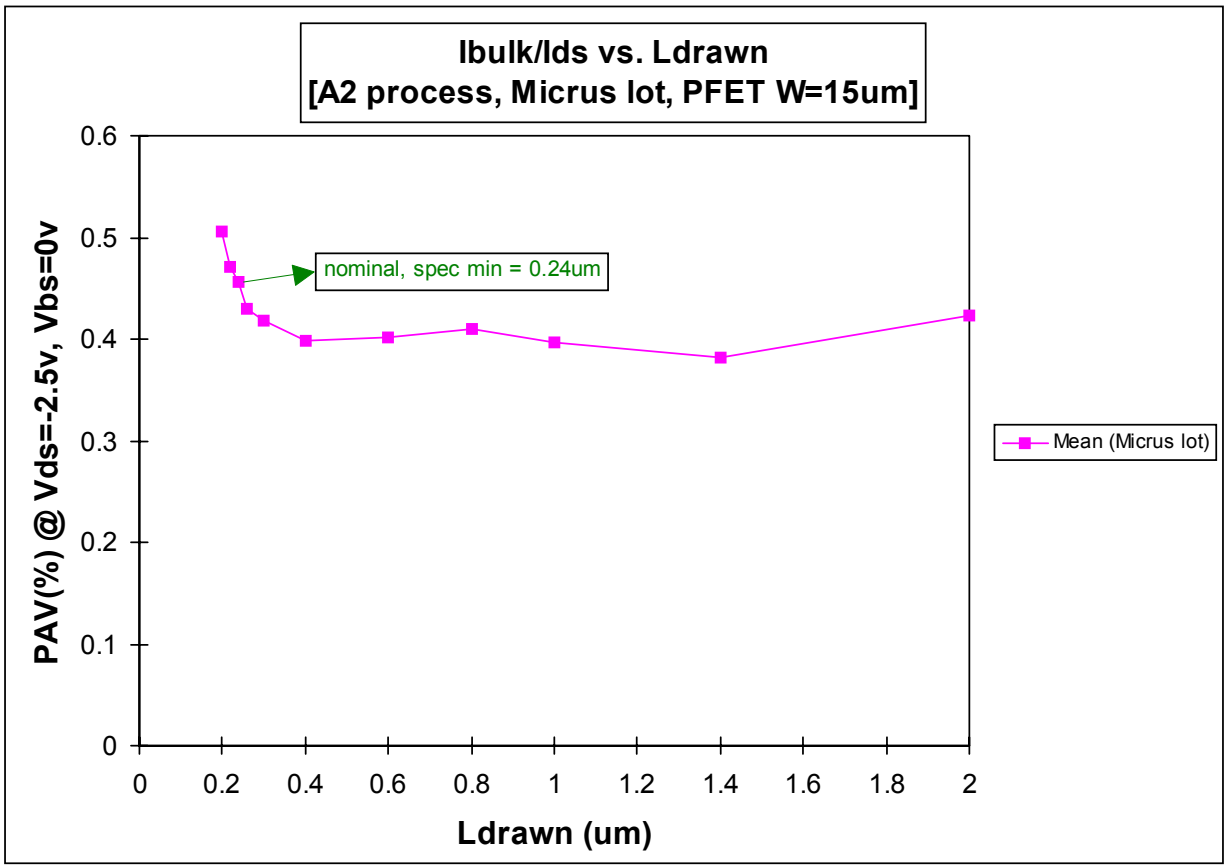
Ibulk/Ids vs. Ldrawn
[A2 process, Micrus lot, PFET W=15um]
PAV(%) @ Vds=-2.5v, Vbs=0v
0.6
0.5
0.4
0.3
0.2
0.1
0
nominal, spec min = 0.24um
Mean (Micrus lot)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Ldrawn (um)

Figure 31

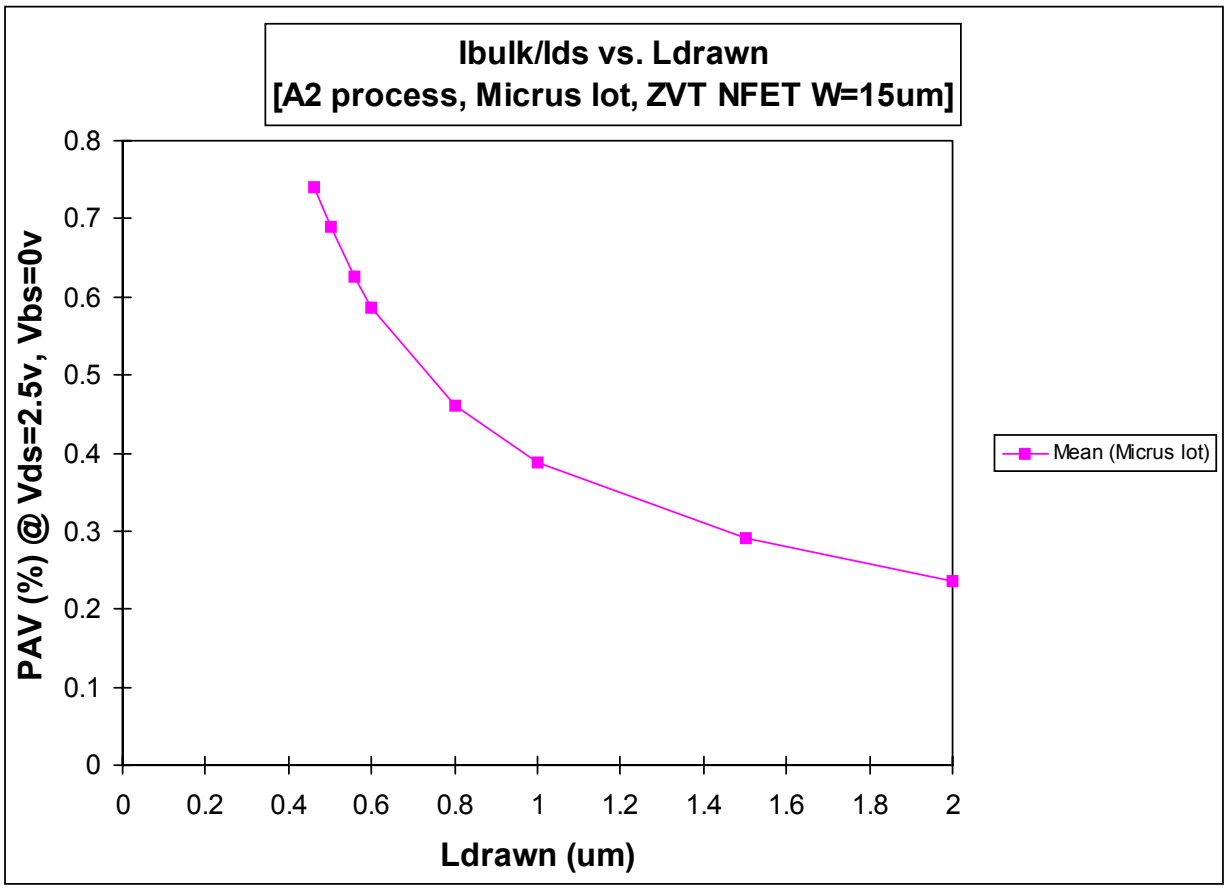
Ibulk/Ids vs. Ldrawn
[A2 process, Micrus lot, ZVT NFET W=15um]
PAV (%) @ Vds=2.5v, Vbs=0v
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Ldrawn (um)
Mean (Micrus lot)

Figure 32

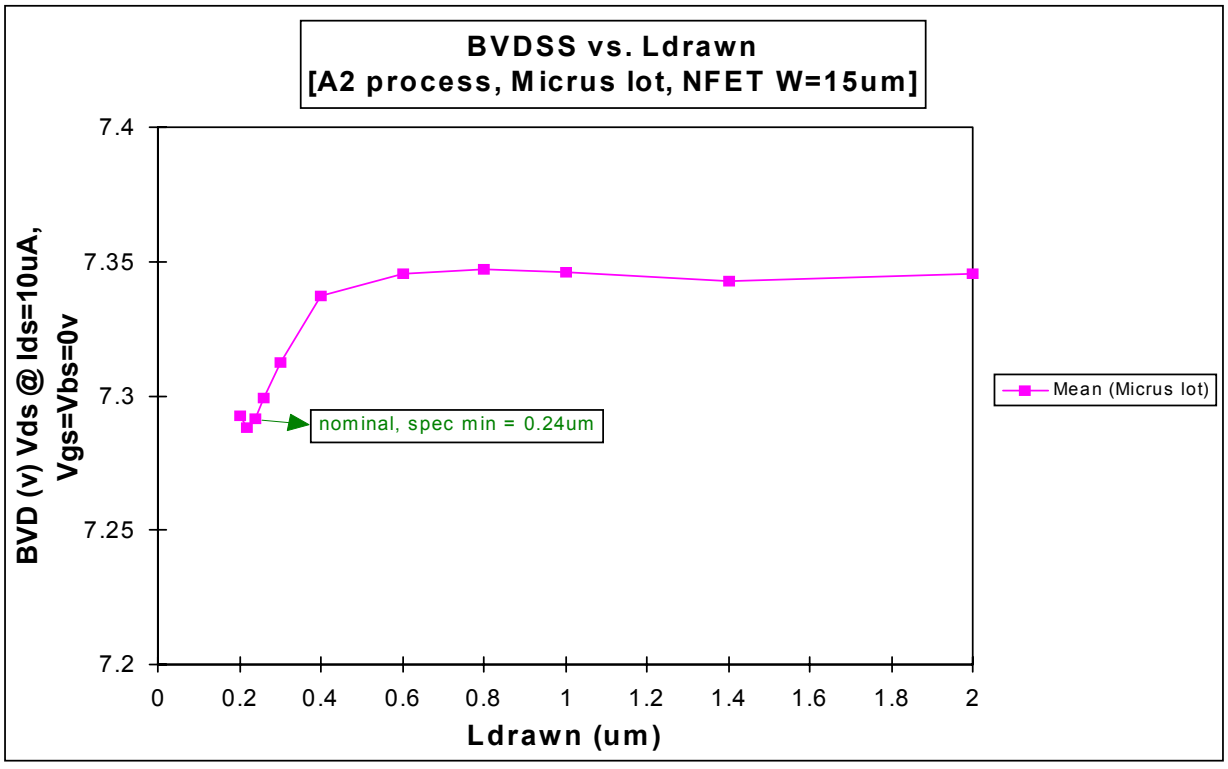
BVDSS vs. Ldrawn
[A2 process, Micrus lot, NFET W=15um]
BVD (v) Vds @ Ids=10uA, Vgs=Vbs=0v
7.4
7.35
7.3
7.25
7.2
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Ldrawn (um)
nominal, spec min = 0.24um
Mean (Micrus lot)

Figure 33

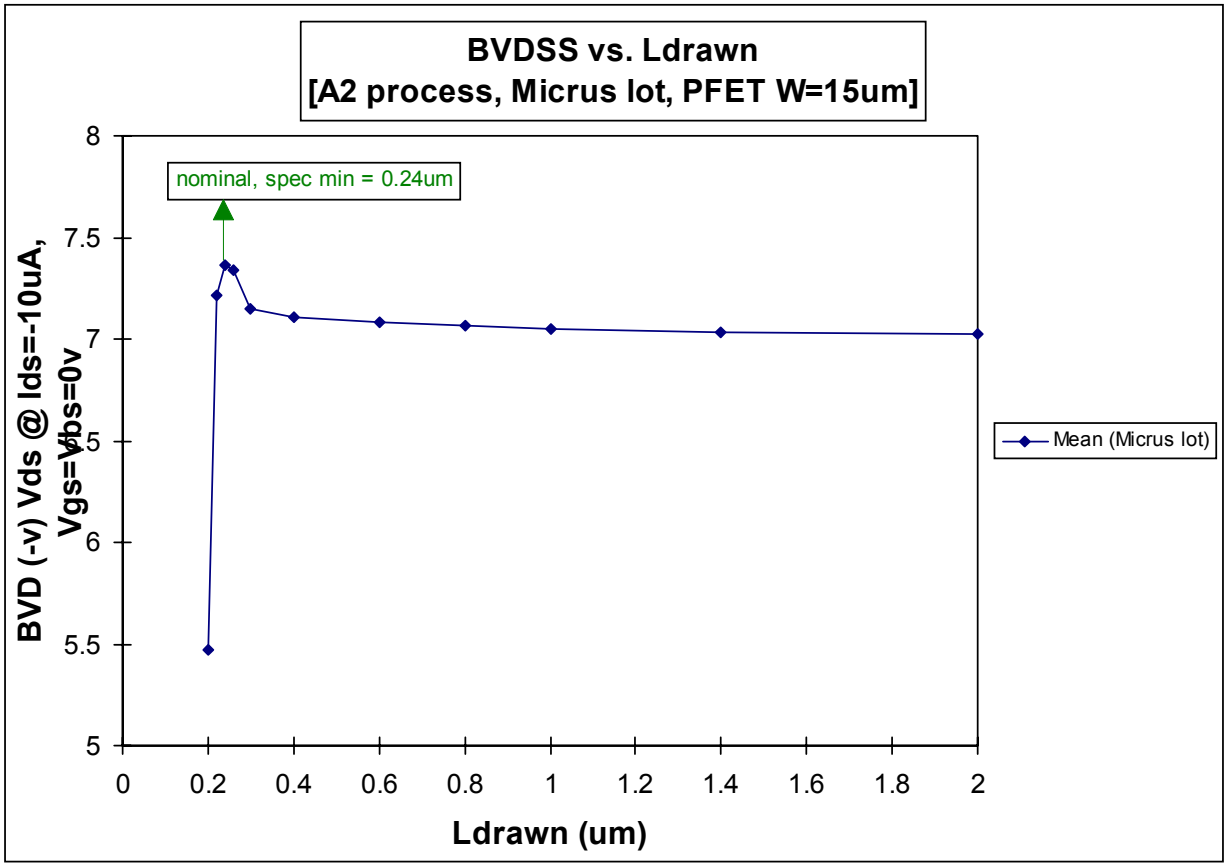

Figure 34

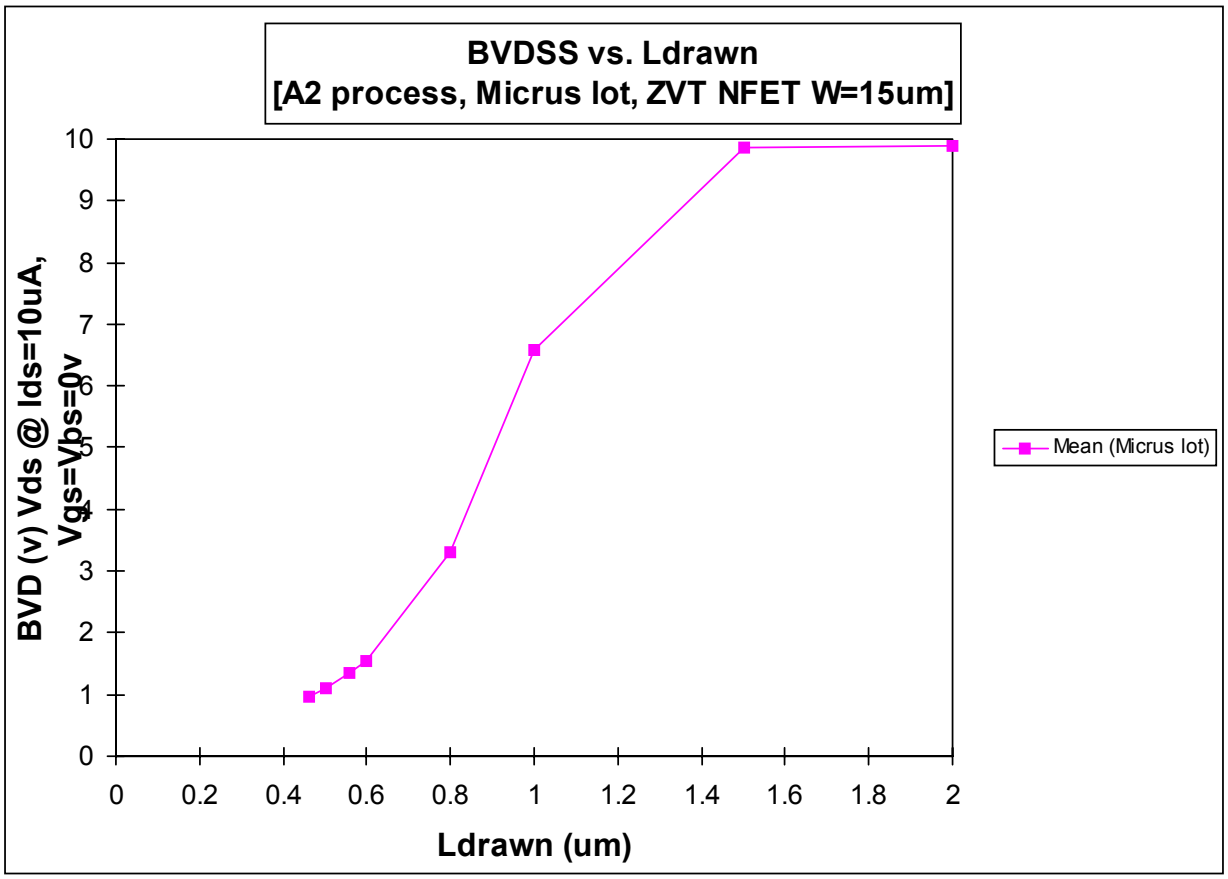
BVDSS vs. Ldrawn
[A2 process, Micrus lot, ZVT NFET W=15um]
BVD (v) Vds @ Ids=10uA, Vgs=Vbs=0v
Ldrawn (um)
Mean (Micrus lot)
0
1
2
3
4
5
6
7
8
9
10
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

Figure 35