Foundry Technology &
Design Infrastructure

LEXX

(L18 Test Chip Catalog)

Sept 2002

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Section **Page**

I. Introduction

This document provides an overview of LEXX that is a test chip for Chartered Semiconductor Manufacture (CSM) Logic 0.18um 1-poly 6-metal salicide 1.8v/3.3v process. The whole chip has a size of 5000μm× 5000μm. It was taped out at September 10, 2002.

In an effort for model qualification, the test chip features several functional circuit blocks such as PLL, Bandgap and current mirror arrays. By monitoring key parameters within these circuits, we will be able to leverage the model performance in circuit level. The test chip also includes transistor modules and resistor modules that serve the vehicles for device characterization and process benchmark. The test chip has also included some special structures that either design groups or Foundry Technology group are interested in. These structures include fuse, 1/f noise, current mirror with gate diode, and NMOS/PMOS capacitors.

Topologically, The chip consists of two major portions. Half of the chip was developed by , which includes device characterization blocks and function circuits. Another half is owned by CSM. It includes the standard modules that interest . CSM has also used this half to test STD cell libraries and pads. Detail information about the test structures can be found in the following chapters.

The Lexx development team includes

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Krish Subramoniam, Mixed Signal Deparment
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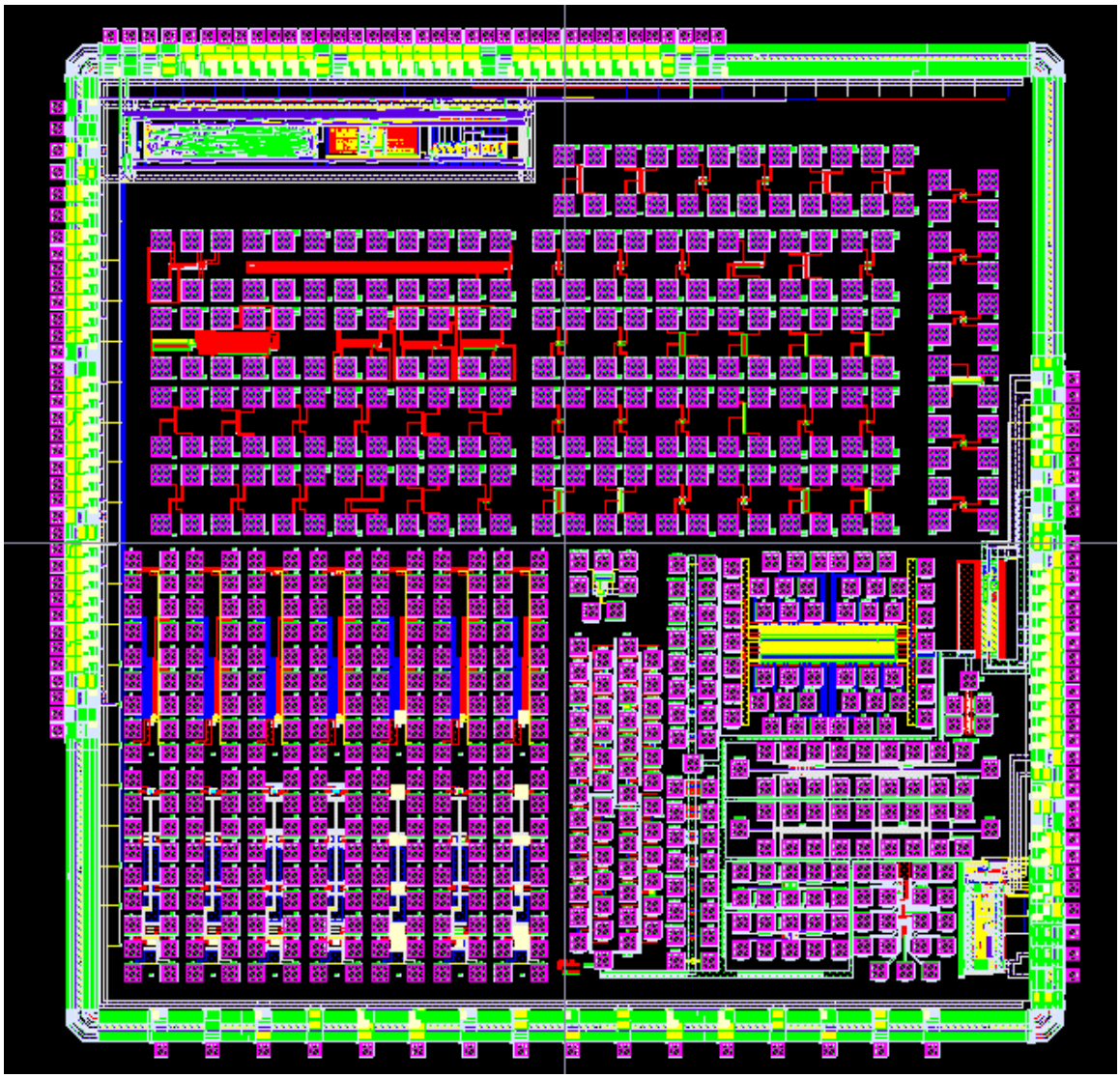
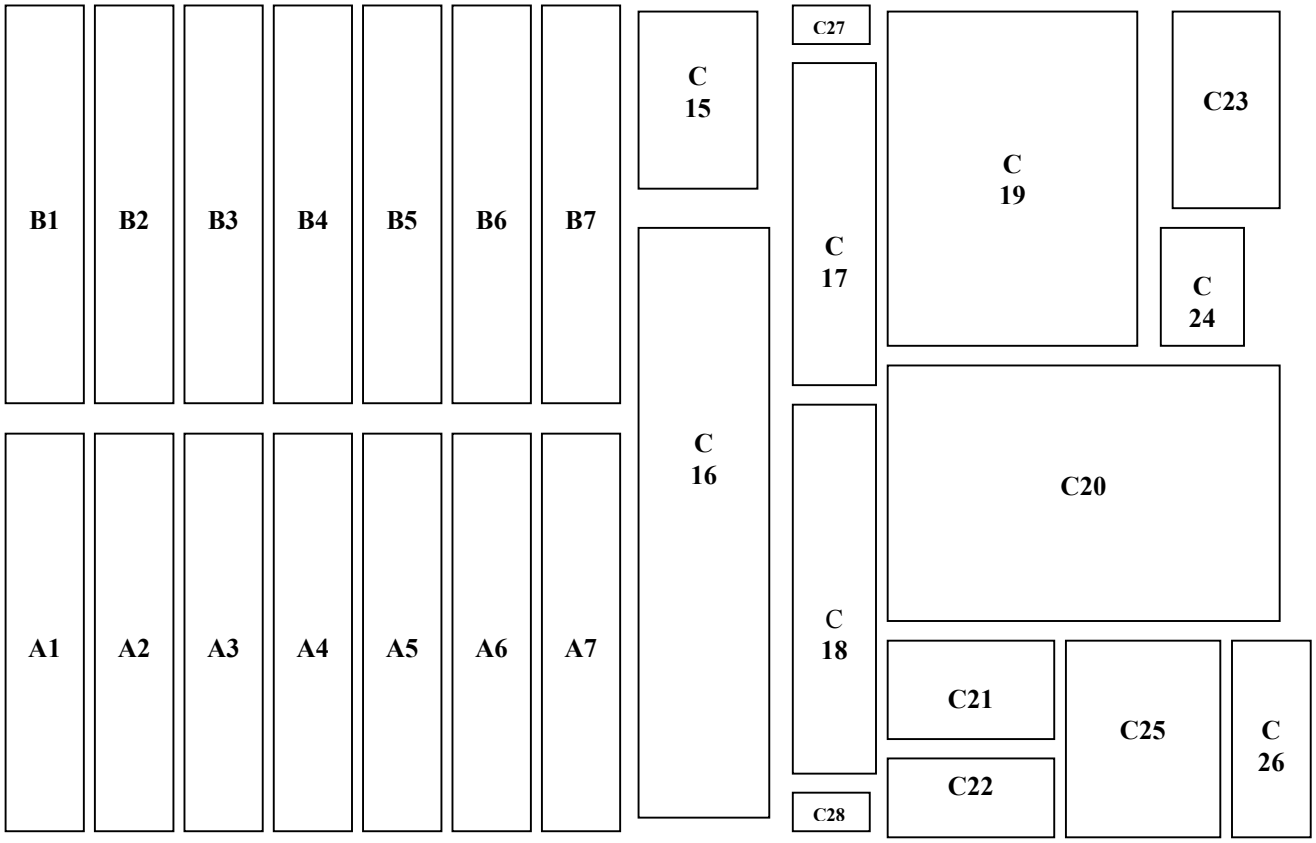


Figure 1, snapshot of the whole chip (5000 × 5000 μm^2)

II, Module Location

1 Module Location of Half

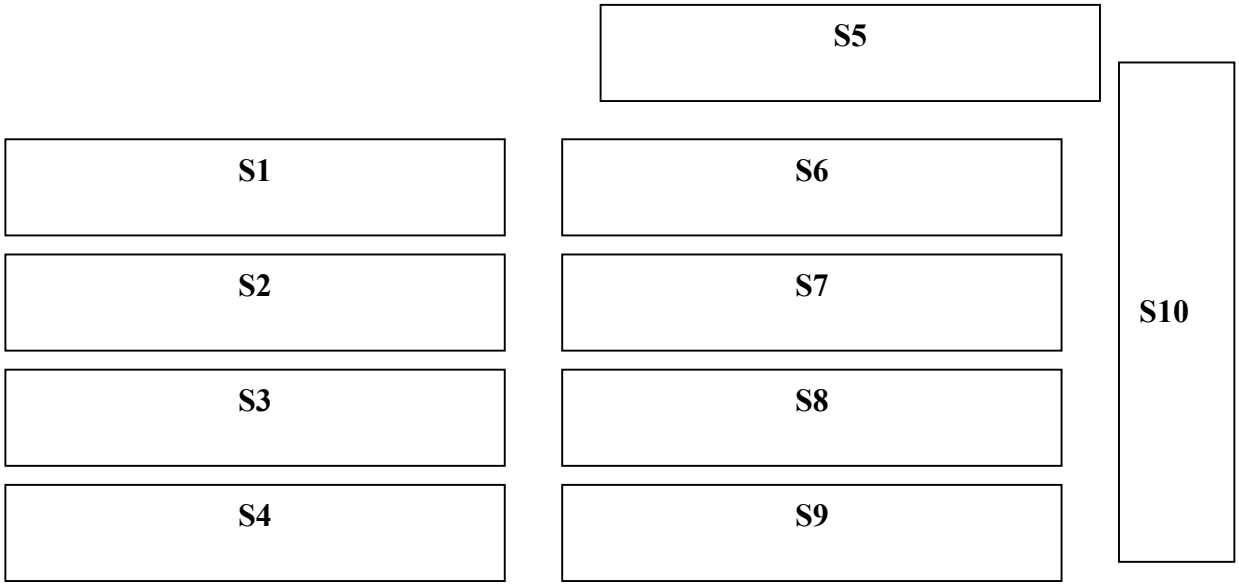


B1, RendNSB
A1, RmatNSB
B2, RendN
A2, RmatN
B3, RendPSB
A3, RmatPSB
B4, RendP
A4, RmatP
B5, RendNW
A5, RmatNW
B6, RenP2NSB
A6, RmaP2NSB
B7, RenP2PSB
A7, RmaP2PSB

C15, Fuse cell
C16, 1/f noise
C17, BJT module without dummies
C18, BJT module with dummies
C19, current mirror array
C20, match gate with diodes
C21, NC and PC module for HV devices
C22, NC and PC module for LV devices
C23, Bandgap bias generator
C24, metal gates
C25, PLL resistor module
C26, PLL.
C27, Finger capacitor
C28, Finger capacitor

Figures 3, Module layout map for half.

2, Module Location of Chartered Half



S1 – CS_RO_mod1
S2 – CS_RO_mod2
S3 – CS_TN_mod1
S4 – CS_TN_mod2
S5 – CS_TP_mod1
S6 – CS_TP_mod2
S7 – CS_TKN_mod1
S8 – CS_TKN_mod2
S9 – CS_TKP_mod1
S10 – CS_TKP_mod2

Figure 2, module layout for Chartered half

3, Pin Assignments of Half

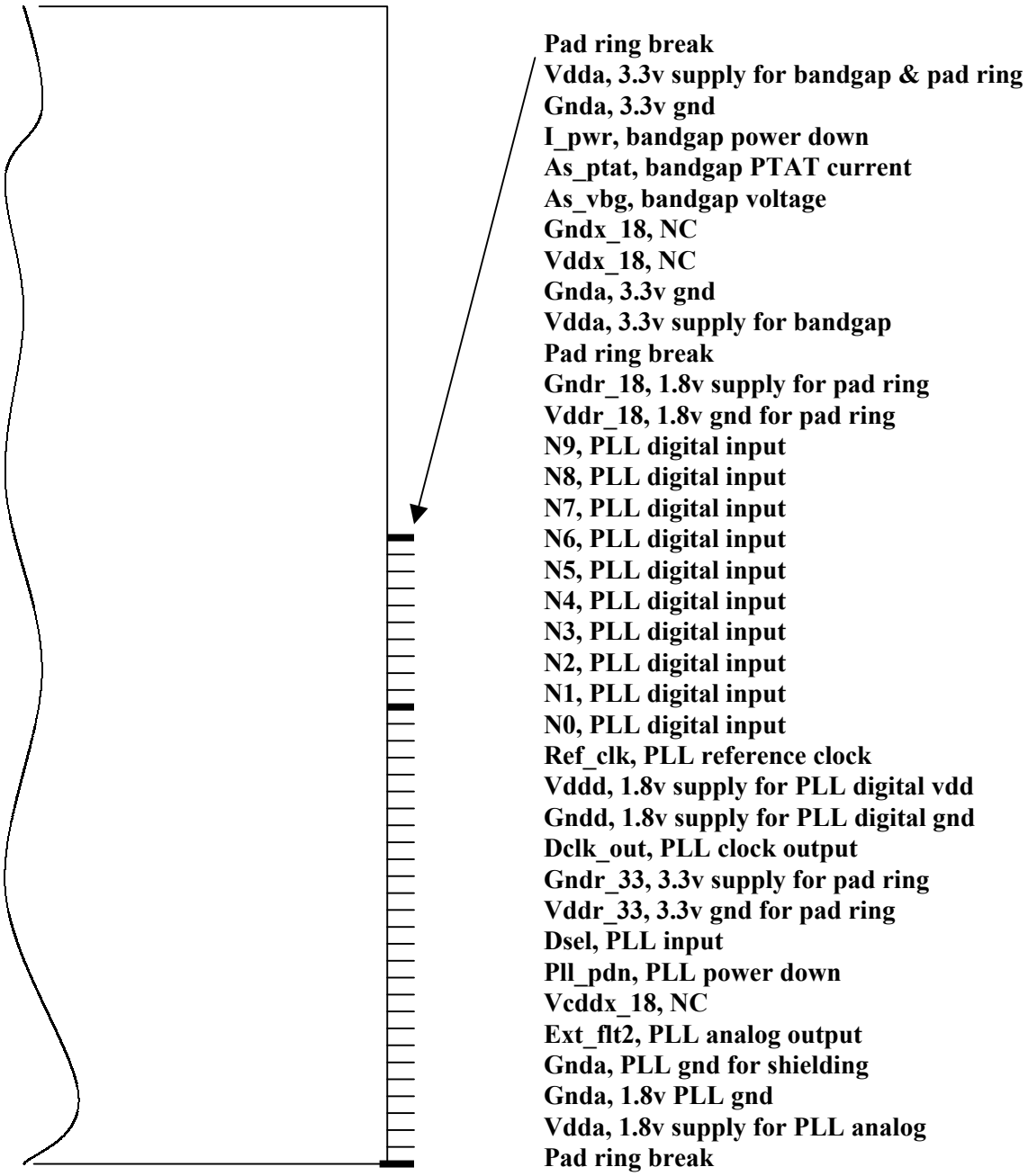


Figure 4, Pin assignment for test structures

III. Function blocks

Location: C26 Name: PLL Size: 200x700um^2

Purpose: To test the new architecture/approach so that we can transition all our plls to a more robust, simple, smaller, faster, and hopefully better jitter performance pll.

Description: Phase-Locked-Loop using 3 stages differential ring oscillator approach and requires no digital calibrations

Pad Assignments:

2 analog output
2 analog power/ground (pll_vdda and pll_gnda)
2 digital power/ground (pll_vddd and pll_gndd)
1 digital output (can support min 50mhz)
1 digital input (can support min 50mhz)
12 digital inputs (static signals)

Note: See figure 4 for more detail PLL pin assignment information.

Location: C19 Name: Mirror Array Size: 900 x 1000 um^2

Purpose: Test matching character vs. distance for different sizes of thick oxide devices schematic

Description: PMOS device array configurable as current mirrors. Contains ten different device sizes each size consisting of 50 2x devices sharing drains and sources.

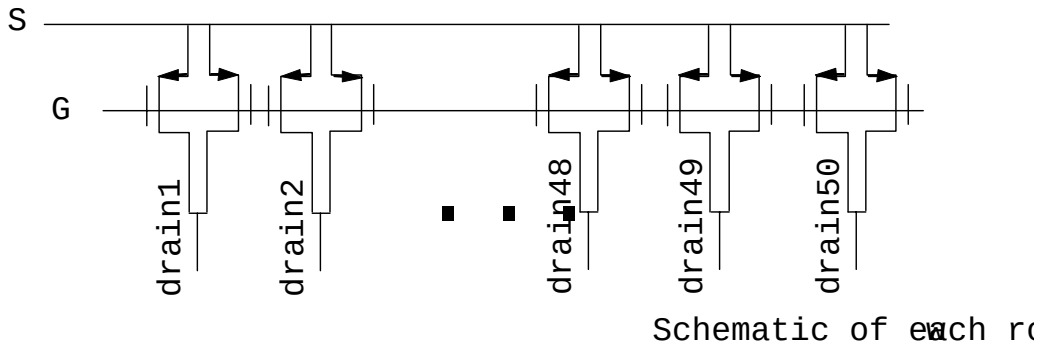


Figure 5, schematic of each row in Mirror Array

Pad Assignment: Sizes shown are for a 1x device. Drains of 2x device are numbered and come out at top and bottom of the array as shown in Fig 6. All devices share a common source which has 4 access points. Gates are shared for each row and are accessible at the sides of the array as shown. Due to space limitations some drains are shared. These are shown as multiple numbers on the pads, each number representing a 2x device.

Location: C23 Name: Band gap size:

Description/purpose: Generates bandgap voltage and supplies PTAT current

Pad Assignment
Outputs are bandgap voltage (as_vbg) and PTAT current (as_iptat).
Inputs: i_pwr (power-on control signal).

The bandgap cell is connected to the padring. See pin diagram for pad locations.

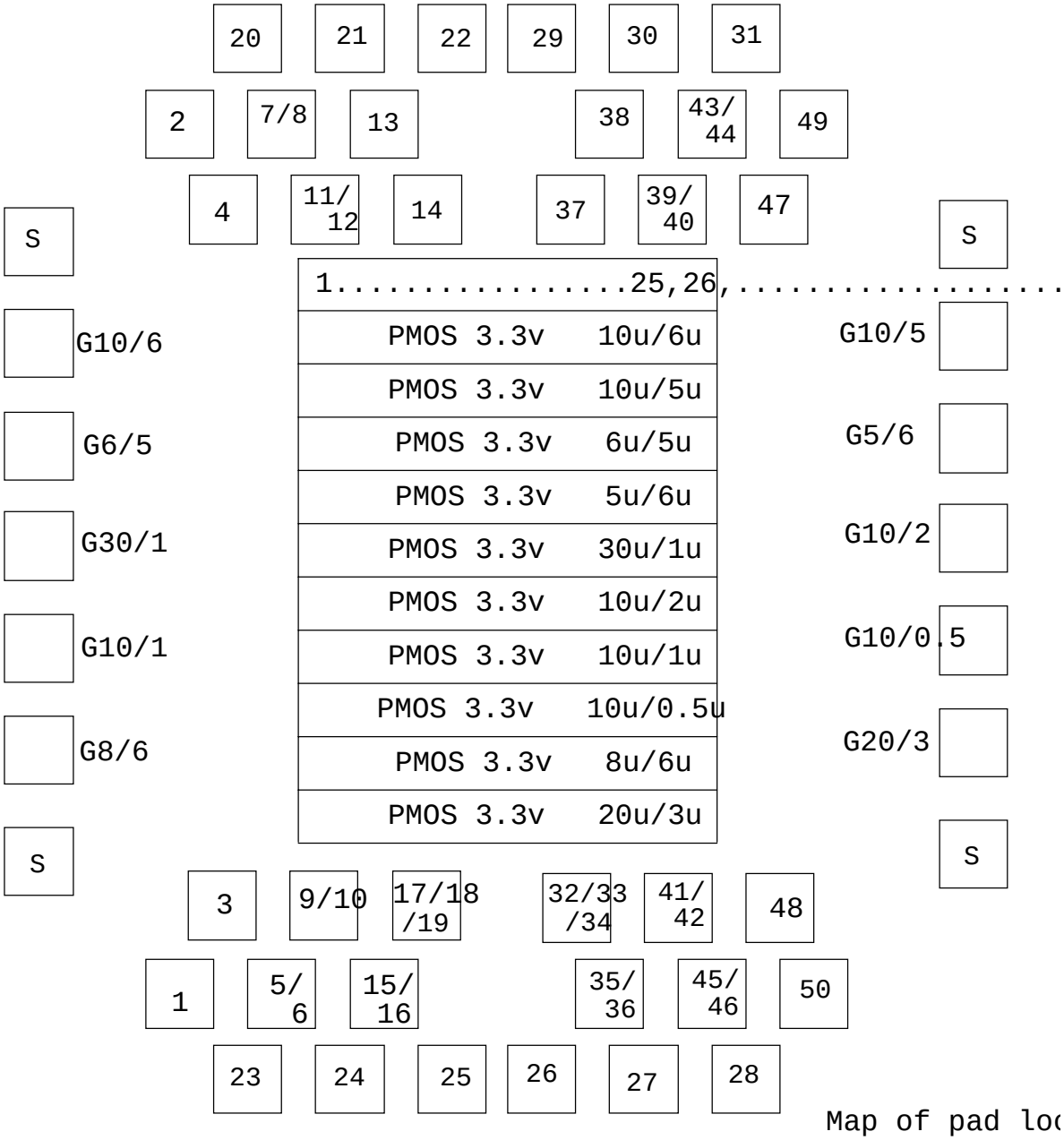


Figure 6, Pad location

Location: C20 **Name: Matching Array w/O Gate Diodes**

Purpose: PMOS device array to test the effects of gate antenna diodes on matching.

Description: Consists of four sizes in four arrays. All devices are thin oxide (1.8V) transistors. Arrays consist of four 2x devices with common gates and sources but independent drains, with antenna diodes on the gates and dummies on each side of the array. Antenna diodes are attached to each individual gate with metal one. As a control there are four of the same size devices without diodes on the gates in each array. Note the devices without diodes share the source with the devices with diodes, but not the gates. Source lines within each section are connected, but, top and bottom sections are independent.
See schematic for connections.
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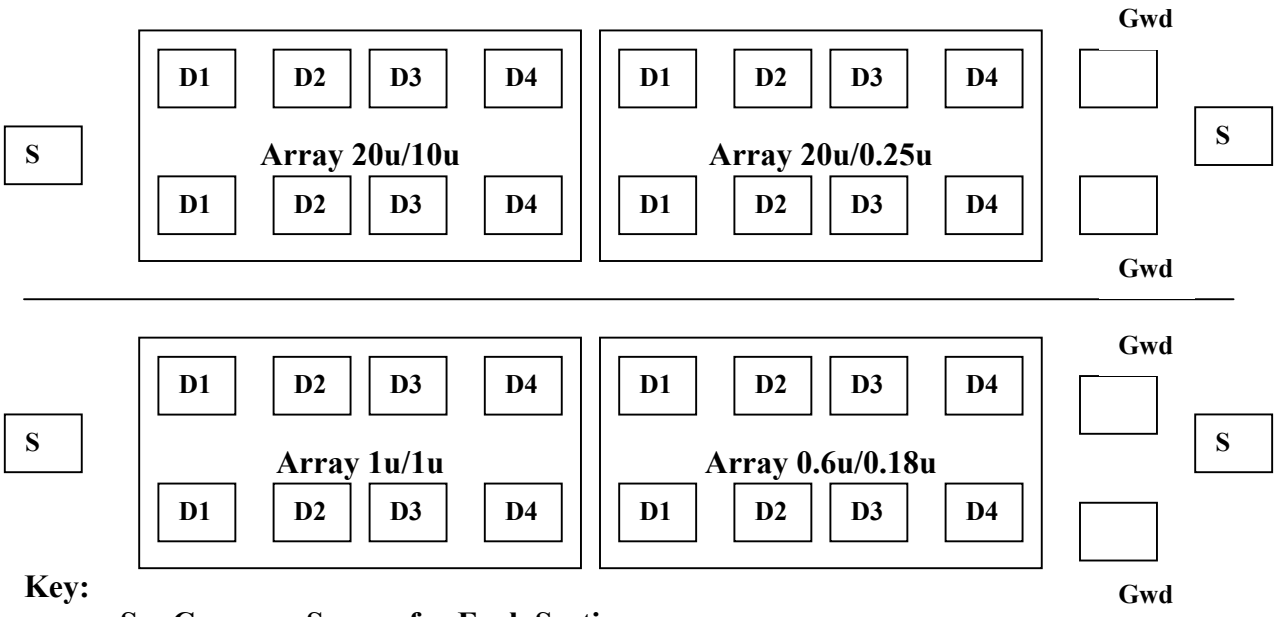


Key:

S = Common Source for Each Section
GwD = Common Gates with Antenna Diodes
GwoD = Common Gates without Antenna Diodes
Dn = Drains of 2x Devices (note: for each section top drain are for devices with anatenna diodes and bottom are without)

Figure 7, Pad location for matching array with gate diode.

Location: C15 Name: Fuse Cell

Purpose: Test metal 4 fuse blowing capability
Description: It includes logic control circuits to address the cell and trigger fuse blow. Output logic senses the status of fuse.

Pad Assignments:

BC Fuse SEL, select the cell
POWER, 3.3v power supply
OUT, Status of fuse. High for fuse blow
BC Fuse EN, Trigger fuse blow when the cell is selected
IDLE PWR, Power enable
BC Fuse MUX, Select between fuse state or logic input
DCND, Ground

Location C16 Name: 1/f noise module

Purpose: measures 1/f noise
Description: The module contains four different geometry devices for each type.

Pad Assignments:

Dev Type	Dev #	Number	Active Width	Gate Length	Drain Pad	Source Pad	Gate Pad	Body Pad
1.8v NMOS	1	1	10	0.18	D18n_1	S18n_1	G18n_1	ground
	2	1	10	1.0	D18n_2	S18n_2	G18n_2	ground
	3	1	10	8	D18n_3	S18n_3	G18n_3	ground
	4	2	5	1	D18n_4	S18n_4	G18n_4	ground
1.8v PMOS	5	1	10	0.18	D18p_1	S18p_1	G18p_1	ground
	6	1	10	1.0	D18p_2	S18p_2	G18p_2	ground
	7	1	10	8	D18p_3	S18p_3	G18p_3	ground
	8	2	5	1	D18p_4	S18p_4	G18p_4	ground
3.3v NMOS	9	1	10	0.18	D33n_1	S33n_1	G33n_1	ground
	10	1	10	1.0	D33n_2	S33n_2	G33n_2	ground
	11	1	10	8	D33n_3	S33n_3	G33n_3	ground
	12	2	5	1	D33n_4	S33n_4	G33n_4	ground
3.3v PMOS	13	1	10	0.18	D33p_1	S33p_1	G33p_1	ground
	14	1	10	1.0	D33p_2	S33p_2	G33p_2	ground
	15	1	10	8	D33p_3	S33p_3	G33p_3	ground
	16	2	5	1	D33p_4	S33p_4	G33p_4	ground

Location: C17 Name: BJT module without dummy

Purpose: Character BJT with different emitter sizes.

Pad Assignments:

Dev #	Name	Emitter Width	Emitter Length	Emitter Pad	Base Pad
1	Min spac	3	3	BJT 3x3 min	BASE
2		3	3	BJT 3x3	BASE
3		5	5	BJT 5x5 min	BASE
4		5	5	BJT5x5	BASE
5		7	7	BJT 7x7	BASE
6		10	10	BJT 10x10	BASE
7		14	14	BJT 14x14	BASE

Location: C18 Name: BJT module with dummies

Purpose: Character BJT with different emitter sizes.

Pad Assignments:

Dev #	Name	Emitter Width	Emitter Length	Emitter Pad	Base Pad
1		3	3	BJT 3x3 min	BASE
2		3	3	BJT 3x3	BASE
3		5	5	BJT 5x5 min	BASE
4		5	5	BJT5x5	BASE
5		7	7	BJT 7x7	BASE
6		10	10	BJT 10x10	BASE
7		14	14	BJT 14x14	BASE

Location: C21 Name: NC/PC of thick oxide devices

Purpose: To measure the characteristics of 3.3v NMOS and PMOS capacitor

Description: There are four different sizes for each type. A “HV” sign at the bottom of the module differentiate it from thin oxide devices.

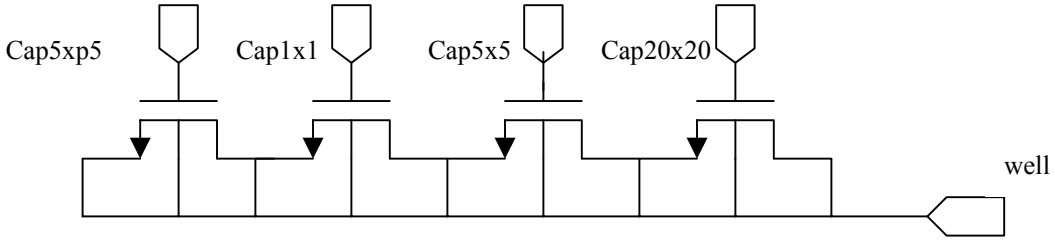


Figure 8, NMOS capacitor test module schematic

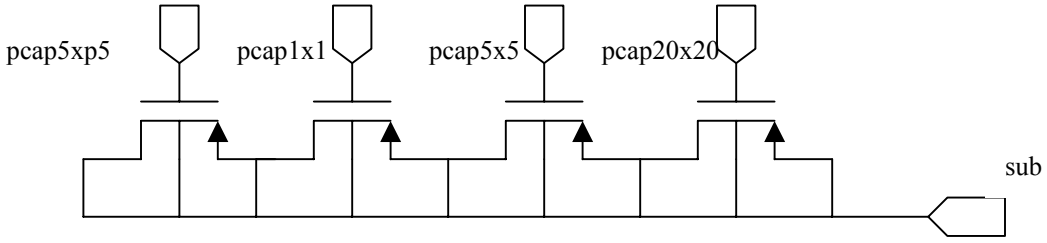


Figure 9, NMOS capacitor test module schematic

Pad Assignments:

	Dev #	Name	Active Width	Gate Length	Drain Pad	Source Pad	Gate Pad	Body Pad
3.3v NMOS	1		0.5	0.5	Well	Well	Cap5xp5	well
	2		1	1	Well	Well	Cap1x1	well
	3		5	5	Well	Well	Cap5x5	well
	4		20	20	Well	Well	Cap20x20	well
3.3v PMOS	5		0.5	0.5	Sub	Sub	Pcap5xp5	Sub
	6		1	1	Sub	Sub	Pcap1x1	Sub
	7		5	5	Sub	Sub	Pcap5x5	Sub
	8		20	20	Sub	Sub	Pcap20x20	sub

Location: C22 Name: NC/PC of thin oxide devices

Purpose: To measure the characteristics of 1.8v NMOS and PMOS capacitor

Description:

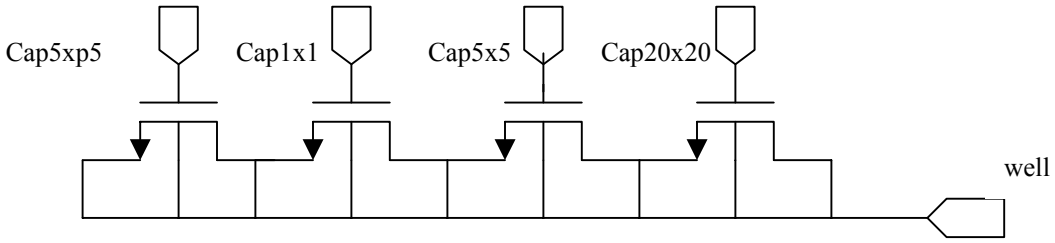


Figure 10, NMOS capacitor test module schematic

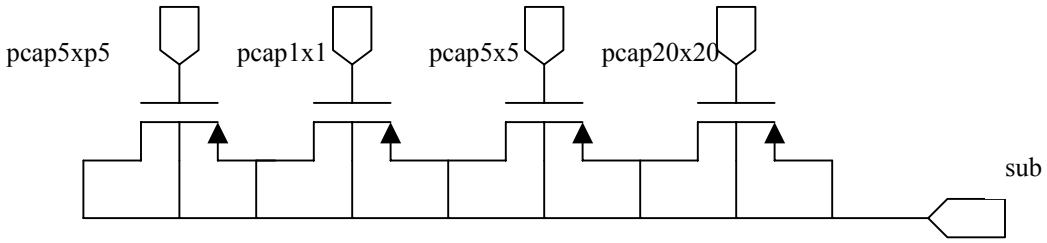


Figure 11, NMOS capacitor test module schematic

Pad Assignments:

	Dev #	Name	Active Width	Gate Length	Drain Pad	Source Pad	Gate Pad	Body Pad
3.3v NMOS	1		0.5	0.5	Well	Well	Cap5xp5	well
	2		1	1	Well	Well	Cap1x1	well
	3		5	5	Well	Well	Cap5x5	well
	4		20	20	Well	Well	Cap20x20	well
3.3v PMOS	5		0.5	0.5	Sub	Sub	Pcap5xp5	Sub
	6		1	1	Sub	Sub	Pcap1x1	Sub
	7		5	5	Sub	Sub	Pcap5x5	Sub
	8		20	20	Sub	Sub	Pcap20x20	sub

Location: C24 Name: Metal Gates

Purpose: To test metal gate characteristics for ESD protection
Description: Two sets of devices with different gate length, and with nwell drain vs non-nwell drain.

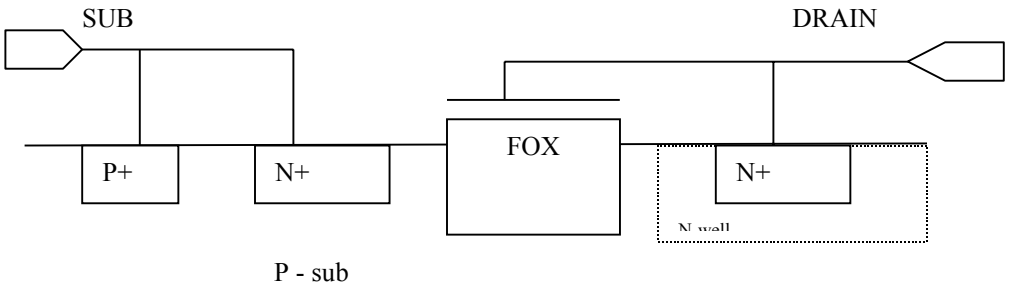


Figure 12, Metal Gate cross-section

Pad Assignments:

Dev #	Name	Active Width	Gate Length	Drain Pad	Source Pad	Gate Pad	Body Pad
1		45	2	M1 2u	SUB	M1 2u	SUB
2		45	3	M2 3u	SUB	M2 3u	SUB
3		45	1.5	M3 1p5u	SUB	M3 1p5u	SUB
4		45	2.5	M4 2p5u	SUB	M4 2p5u	SUB

Location: C25 Name: PLL resistor module

Purpose: To test Rend and Δw effect for N+ poly resister.
Description: There are three N+ poly resistor bars with same L/W ratio.

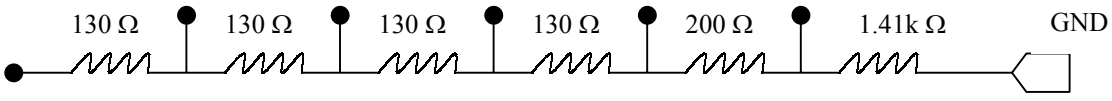


Figure 13, N+ poly resistor schematic

Location: C27 / C28 Name: muti-finger capacitor

Purpose: To test the characteristics of metal to metal multi-finger capacitors

Description:

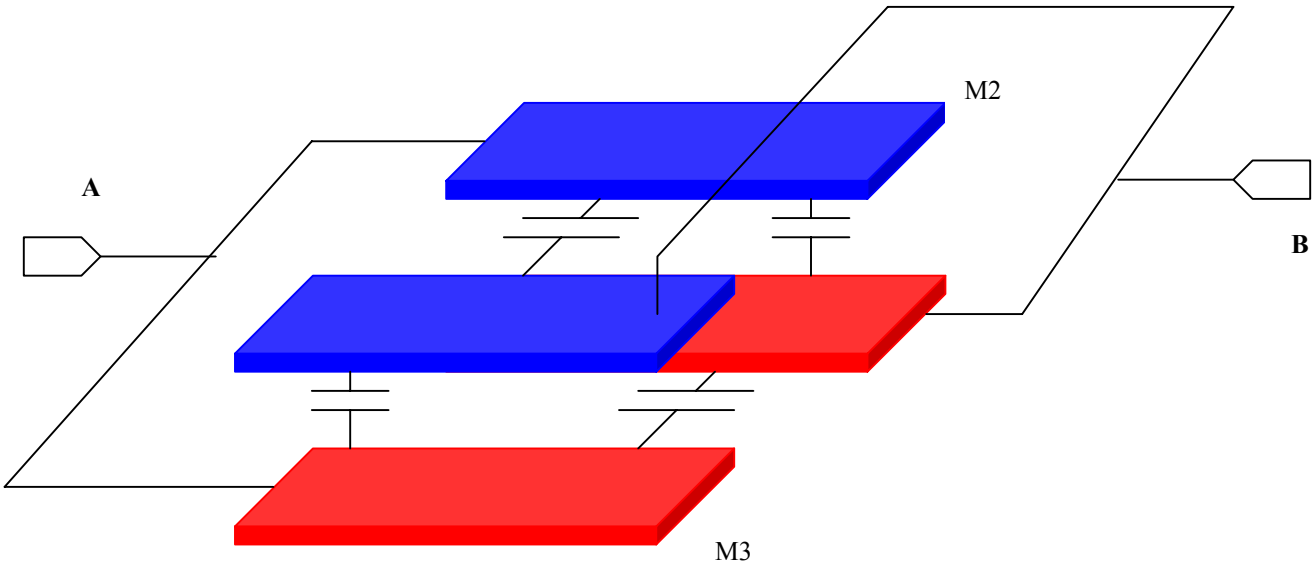


Figure 14, Muti-finger capacitor structure

Pad Assignments:

Dev #	Name	M3 Width	M3 Length	M2 width	M2 length	M2 to M3 space	M2 to M2 space	M3 to M3 space
1		10	10	1	6	7		5
2		5	10	2	6	7		5

IV. Device characterization:

Modules of type Rmat and Rend are used in pairs to acquire Resistor parameters such as Rsheet, deltaW, tcr1, tcr2, vcr1, vcr2, vbak1, vbak2, Rcon, Rint/Rend and matching .

Location: A1 Name: RmatNSB, N+ diffused Salicide blocked

General Description:

This 18 pad module contains 3 sets of 4 matched resistors, each set representing one resistor width. Two of the resistors for each width are surrounded by 'dummy' resistors, the other two are not so protected. This module also contains a VanderPauw sheet resistance monitor for this type resistor.

Specifics:

N+ diffused Salicide blocked Resistor layer. Pad 10 provides backside substrate contact for backbias.

Res Group A: W=4um, Lsalblk=20um, Lend=0.7um, Num contacts/end=8.
Res Group B: W=1um, Lsalblk=5um, Lend=0.7um, Num contacts/end=2.
Res Group C: W=9um, Lsalblk=45um, Lend=0.7um, Num contacts/end=17.

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	VDP I+			18	VDP V+	
2	VDP I-			17	VDP V-	
3	Ra1d	W=4, Lsb=20, Lend=0.7, Nc=8		16	Ra3	
4	Ra2d			15	Ra4	
5	Rb1d	W=1, Lsb=5, Lend=0.7, Nc=2		14	Rb3	
6	Rb2d			13	Rb4	
7	Rc1d	W=9, Lsb=45. Lend=0.7, Nc=17		12	Rc3	
8	Rc2d			11	Rc4	
9	Res Com			10	Sub COM	

Diagram:

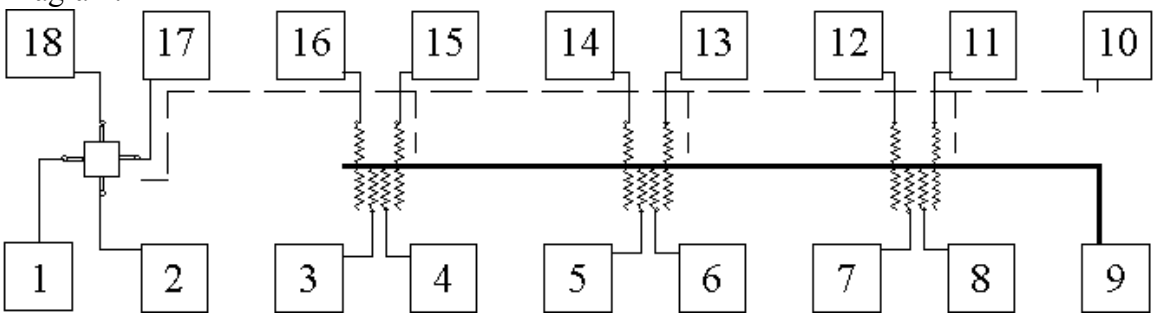


Figure 15, RmatNSB, N+ diffused Salicide blocked

Location: B1 Name: RendN, N+ diffused Salicide Block

General Description:

This 18 pad module contains three 3-tap resistors, each having different widths. Resistors are of the same overall length and each tap on each resistor is in the same relative position on the resistors. Each of these resistors also have separate Current In (I+) terminals and share one Current Out (common I-) terminal. This module also contains a single-contact Kelvin-type test structure.

Specifics:

N+ diffused salicide block Resistor layer. Pad 10 provides backside substrate contact for backbias. Drawn contact size 0.22x0.22um.

3-Tap Res A: W=1um, L1=0.51um, L2=3.01um, L3=27.42um, Lend=0.7um, Ws=0.4um, Nc=2

3-Tap Res B: W=4um, L1=0.5um, L2=3.0um, L3=27.5um, Lend=0.7um, Ws=0.4um, Nc=8

3-Tap Res C: W=9um, L1=0.5um, L2=3.0um, L3=27.5um, Lend=0.7um, Ws=0.4um, Nc=17

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	Con I+	Single Kelvin Contact		18	Con V-	
2	Con V+			17	Con I-	
3	Ratap2	3-Tap Resistor A (1um)		16	Ratap3	
4	Ratap1			15	Ra I+	
5	Rbtap2	3-Tap Resistor B(4um)		14	Rbtap3	
6	Rbtap1			13	Rb I+	
7	Rctap2	3-Tap Resistor C(9um)		12	Rctap3	
8	Rctap1			11	Rc I+	
9	Res Com I-			10	Sub COM	

Diagram:

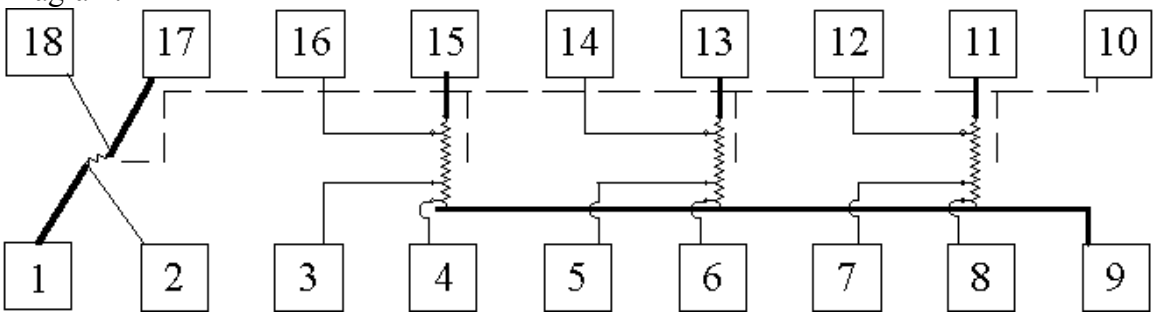


Figure 16, RendN, N+ diffused Salicide Block

Location: A2 Name: RmatN, N+ diffused

General Description:

This 18 pad module contains 3 sets of 4 matched resistors, each set representing one resistor width. Two of the resistors for each width are surrounded by 'dummy' resistors, the other two are not so protected. This module also contains a VanderPauw sheet resistance monitor for this type resistor.

Specifics:

N+ diffused Resistor layer. Pad 10 provides backside substrate contact for backbias.

Res Group A: W=4um, Lcc=20.44um, Lend=0.48um, Num contacts/end=8.
Res Group B: W=1um, Lcc=5.44um, Lend=0.48um, Num contacts/end=2.
Res Group C: W=9um, Lcc=45.44um, Lend=0.48um, Num contacts/end=17.

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	VDP I+			18	VDP V+	
2	VDP I-			17	VDP V-	
3	Ra1d	W=4, Lcc=20.44, Lend=0.48, Nc=8		16	Ra3	
4	Ra2d			15	Ra4	
5	Rb1d	W=1, Lcc=5.44, Lend=0.48, Nc=2		14	Rb3	
6	Rb2d			13	Rb4	
7	Rc1d	W=9, Lcc=45.44, Lend=0.48, Nc=17		12	Rc3	
8	Rc2d			11	Rc4	
9	Res Com			10	Sub COM	

Diagram:

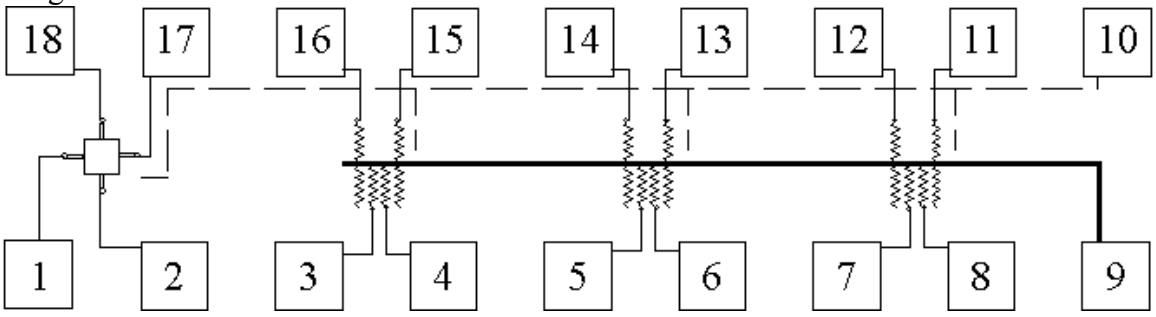


Figure 17, RmatN, N+ diffused

Location: B2 Name: RendN, N+ diffused

General Description:

This 18 pad module contains three 3-tap resistors, each having different widths. Resistors are of the same overall length and each tap on each resistor is in the same relative position on the resistors. Each of these resistors also have separate Current In (I+) terminals and share one Current Out (common I-) terminal. This module also contains a single-contact Kelvin-type test structure.

Specifics:

N+ diffused Resistor layer. Pad 10 provides backside substrate contact for backbias. Drawn contact size 0.22x0.22um. Distances to inside of contact edge.

3-Tap Res A: W=1um, L1=0.73um, L2=3.23um, L3=27.64um, Lend=0.48um, Ws=0.4um, Nc=2

3-Tap Res B: W=4um, L1=0.72um, L2=3.22um, L3=27.72um, Lend=0.48um, Ws=0.4um, Nc=8

3-Tap Res C: W=9um, L1=0.72um, L2=3.22um, L3=27.72um, Lend=0.48um, Ws=0.4um, Nc=17

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	Con I+	Single Kelvin Contact		18	Con V-	
2	Con V+			17	Con I-	
3	Ratap2	3-Tap Resistor A (1um)		16	Ratap3	
4	Ratap1			15	Ra I+	
5	Rbtap2	3-Tap Resistor B(4um)		14	Rbtap3	
6	Rbtap1			13	Rb I+	
7	Rctap2	3-Tap Resistor C(9um)		12	Rctap3	
8	Rctap1			11	Rc I+	
9	Res Com I-			10	Sub COM	

Diagram:

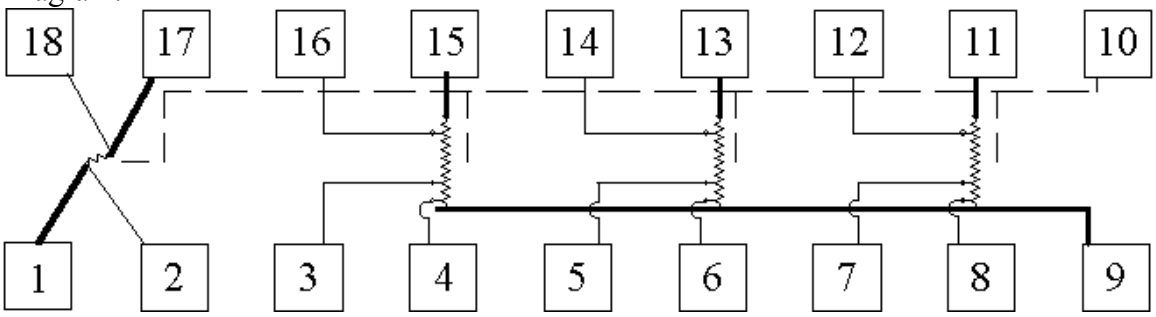


Figure 18, RendN, N+ diffused

Location: A3 Name: RmatPSB, P+ diffused Salicide Block

General Description:

This 18 pad module contains 3 sets of 4 matched resistors, each set representing one resistor width. Two of the resistors for each width are surrounded by 'dummy' resistors, the other two are not so protected. This module also contains a VanderPauw sheet resistance monitor for this type resistor.

Specifics:

P+ diffused Salicide Block Resistor layer. Pad 10 provides Nwell contact for backbias.

Res Group A: W=4um, Lsalblk=20um, Lend=0.7um, Num contacts/end=8.
Res Group B: W=1um, Lsalblk=5um, Lend=0.7um, Num contacts/end=2.
Res Group C: W=9um, Lsalblk=45um, Lend=0.7um, Num contacts/end=17.

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	VDP I+			18	VDP V+	
2	VDP I-			17	VDP V-	
3	Ra1d	W=4, Lsb=20, Lend=0.7, Nc=8		16	Ra3	
4	Ra2d			15	Ra4	
5	Rb1d	W=1, Lsb=5, Lend=0.7, Nc=2		14	Rb3	
6	Rb2d			13	Rb4	
7	Rc1d	W=9, Lsb=45. Lend=0.7, Nc=17		12	Rc3	
8	Rc2d			11	Rc4	
9	Res Com			10	NW COM	

Diagram:

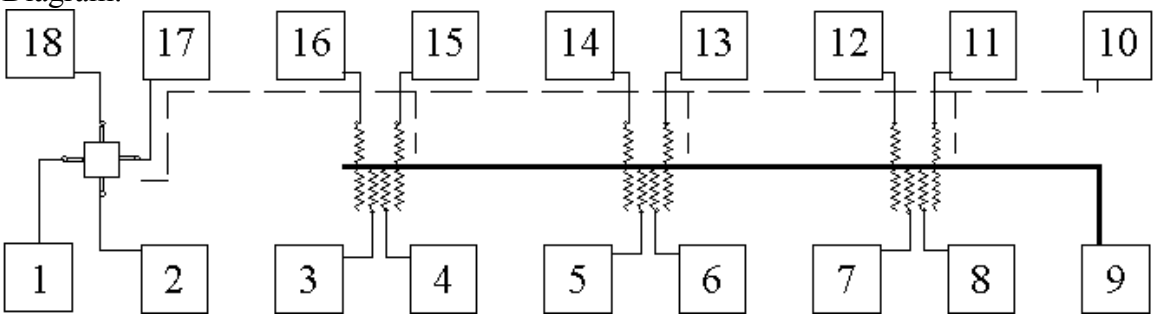


Figure 19, RmatPSB, P+ diffused Salicide Block

Location: B3 Name: RendPSB, P+ diffused Salicide Blocked

General Description:

This 18 pad module contains three 3-tap resistors, each having different widths. Resistors are of the same overall length and each tap on each resistor is in the same relative position on the resistors. Each of these resistors also have separate Current In (I+) terminals and share one Current Out (common I-) terminal. This module also contains a single-contact Kelvin-type test structure.

Specifics:

P+ diffused Salicide Block Resistor layer. Pad 10 provides Nwell contact for backbias. Drawn contact size 0.22x0.22um.

3-Tap Res A: W=1um, L1=0.51um, L2=3.01um, L3=27.42um, Lend=0.7um, Ws=0.4um, Nc=2

3-Tap Res B: W=4um, L1=0.5um, L2=3.0um, L3=27.5um, Lend=0.7um, Ws=0.4um, Nc=8

3-Tap Res C: W=9um, L1=0.5um, L2=3.0um, L3=27.5um, Lend=0.7um, Ws=0.4um, Nc=17

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	Con I+	Single Kelvin Contact		18	Con V-	
2	Con V+			17	Con I-	
3	Ratap2	3-Tap Resistor A (1um)		16	Ratap3	
4	Ratap1			15	Ra I+	
5	Rbtap2	3-Tap Resistor B(4um)		14	Rbtap3	
6	Rbtap1			13	Rb I+	
7	Rctap2	3-Tap Resistor C(9um)		12	Rctap3	
8	Rctap1			11	Rc I+	
9	Res Com I-			10	NW COM	

Diagram:

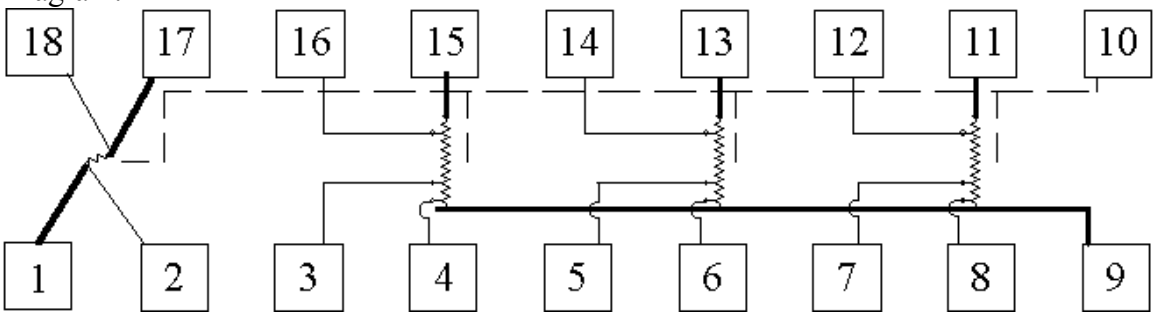


Figure 20, RendPSB, P+ diffused Salicide Blocked

Location: A4 Name: RmatP, P+ diffused

General Description:

This 18 pad module contains 3 sets of 4 matched resistors, each set representing one resistor width. Two of the resistors for each width are surrounded by 'dummy' resistors, the other two are not so protected. This module also contains a VanderPauw sheet resistance monitor for this type resistor.

Specifics:

P+ diffused Resistor layer. Pad 10 provides Nwell contact for backbias.

Res Group A: W=4um, Lcc=20.44um, Lend=0.48um, Num contacts/end=8.
Res Group B: W=1um, Lcc=5.44um, Lend=0.48um, Num contacts/end=2.
Res Group C: W=9um, Lcc=45.44um, Lend=0.48um, Num contacts/end=17.

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	VDP I+			18	VDP V+	
2	VDP I-			17	VDP V-	
3	Ra1d	W=4, Lcc=20.44, Lend=0.48, Nc=8		16	Ra3	
4	Ra2d			15	Ra4	
5	Rb1d	W=1, Lcc=5.44, Lend=0.48, Nc=2		14	Rb3	
6	Rb2d			13	Rb4	
7	Rc1d	W=9, Lcc=45.44, Lend=0.48, Nc=17		12	Rc3	
8	Rc2d			11	Rc4	
9	Res Com			10	NW COM	

Diagram:

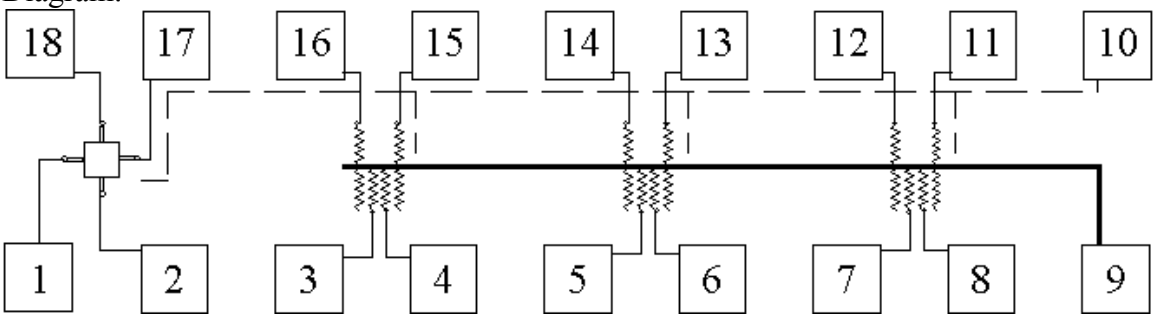


Figure 21, RmatP, P+ diffused

Location: B4 Name: RendP, P+ diffused

General Description:

This 18 pad module contains three 3-tap resistors, each having different widths. Resistors are of the same overall length and each tap on each resistor is in the same relative position on the resistors. Each of these resistors also have separate Current In (I+) terminals and share one Current Out (common I-) terminal. This module also contains a single-contact Kelvin-type test structure.

Specifics:

P+ diffused Resistor layer. Pad 10 provides Nwell contact for backbias. Drawn contact size 0.22x0.22um.

3-Tap Res A: W=1um, L1=0.73um, L2=3.23um, L3=27.64um, Lend=0.48um, Ws=0.4um, Nc=2

3-Tap Res B: W=4um, L1=0.72um, L2=3.22um, L3=27.72um, Lend=0.48um, Ws=0.4um, Nc=8

3-Tap Res C: W=9um, L1=0.72um, L2=3.22um, L3=27.72um, Lend=0.48um, Ws=0.4um, Nc=17

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	Con I+	Single Kelvin Contact		18	Con V-	
2	Con V+			17	Con I-	
3	Ratap2	3-Tap Resistor A (1um)		16	Ratap3	
4	Ratap1			15	Ra I+	
5	Rbtap2	3-Tap Resistor B(4um)		14	Rbtap3	
6	Rbtap1			13	Rb I+	
7	Rctap2	3-Tap Resistor C(9um)		12	Rctap3	
8	Rctap1			11	Rc I+	
9	Res Com I-			10	NW COM	

Diagram:

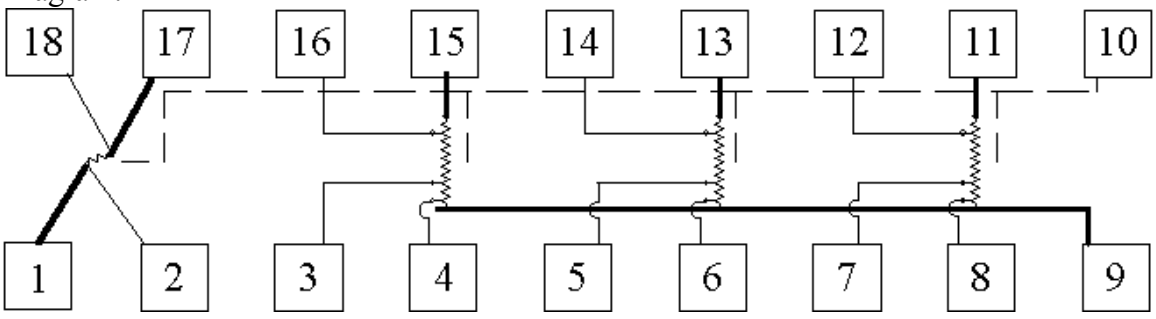


Figure 22, RendP, P+ diffused

Location: A5 Name: RmatNW, NW under STI

General Description:

This 18 pad module contains 3 sets of 4 matched resistors, each set representing one resistor width. Two of the resistors for each width are surrounded by 'dummy' resistors, the other two are not so protected. This module also contains a VanderPauw sheet resistance monitor for this type resistor.

Specifics:

NW under STI Resistor layer. Pad 10 provides backside substrate contact for backbias. Lengths measured from inner N+ AA edge.

Res Group A: W=4.um, Laa=20.3um, Lend=0.69um, Num contacts/end=7.
Res Group B: W=2.2um, Laa=11.3um, Lend=0.69um, Num contacts/end=4
Res Group C: W=9um, Laa=45.45um, Lend=0.54um, Num contacts/end=17.

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	VDP I+	16 x 16 um VDP		18	VDP V+	
2	VDP I-			17	VDP V-	
3	Ra1d	W=4, Laa=20.3, Lend=0.69, Nc=7		16	Ra3	
4	Ra2d			15	Ra4	
5	Rb1d	W=2.2, Laa=11.3 Lend=0.69, Nc=4		14	Rb3	
6	Rb2d			13	Rb4	
7	Rc1d	W=9, Lsb=45.45. Lend=0.54, Nc=17		12	Rc3	
8	Rc2d			11	Rc4	
9	Res Com			10	Sub COM	

Diagram:

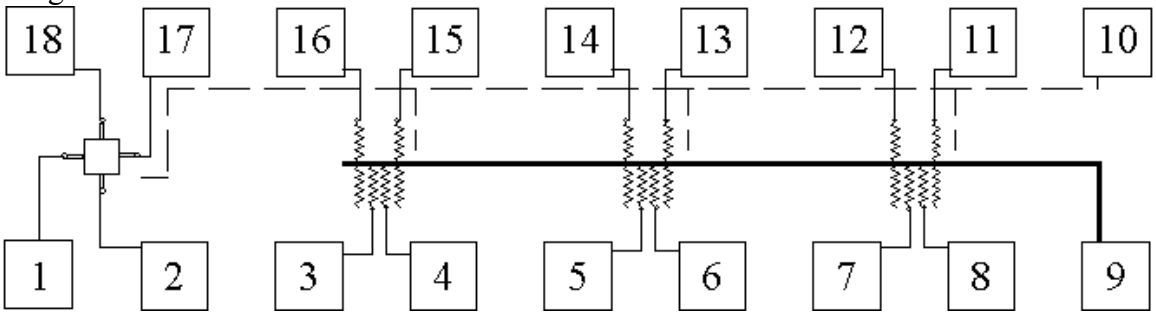


Figure 23, RmatNW, NW under STI

Location: B5 Name: RendNW, NW under STI

General Description:

This 18 pad module contains three 3-tap resistors, each having different widths. Resistors are of the same overall length and each tap on each resistor is in the same relative position on the resistors. Each of these resistors also have separate Current In (I+) terminals and share one Current Out (common I-) terminal. This module also contains a single-contact Kelvin-type test structure.

Specifics:

NW under STI Resistor layer. Pad 10 provides backside substrate contact for backbias. Drawn contact size 0.22x0.22um. Lengths measured from inner AA edge.

3-Tap Res A: W=2.2um, L1=1.56um, L2=4.36um, L3=28.47um, Lend=0.69um, Ws=2.2um, Nc=3

3-Tap Res B: W=4um, L1=1.55um, L2=4.35um, L3=28.55um, Lend=0.69um, Ws=2.2um, Nc=7

3-Tap Res C: W=9um, L1=1.555um, L2=4.36um, L3=28.55um, Lend=0.69um, Ws=2.2um~, Nc=16

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	Con I+	Single Kelvin Contact		18	Con V-	
2	Con V+			17	Con I-	
3	Ratap2	3-Tap Resistor A (1um)		16	Ratap3	
4	Ratap1			15	Ra I+	
5	Rbtap2	3-Tap Resistor B(4um)		14	Rbtap3	
6	Rbtap1			13	Rb I+	
7	Rctap2	3-Tap Resistor C(9um)		12	Rctap3	
8	Rctap1			11	Rc I+	
9	Res Com I-			10	Sub COM	

Diagram:

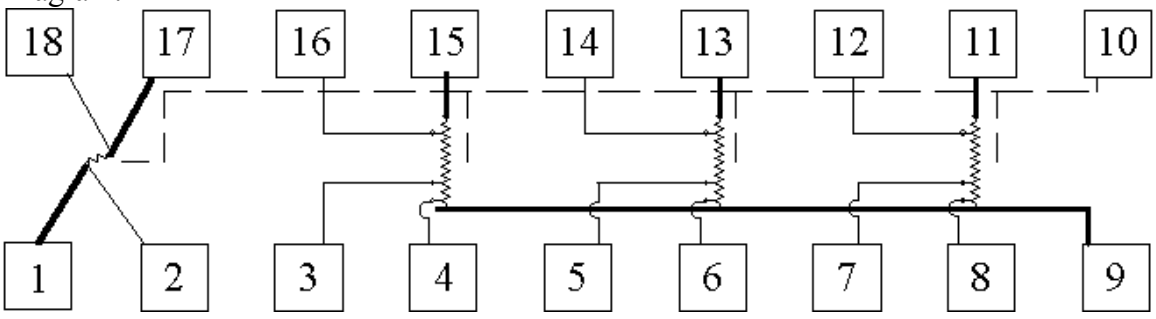


Figure 24, RendNW, NW under STI

Location: A6 Name: RmatP2NSB, N+ Poly Silicide Blocked

General Description:

This 18 pad module contains 3 sets of 4 matched resistors, each set representing one resistor width. Two of the resistors for each width are surrounded by 'dummy' resistors, the other two are not so protected. This module also contains a VanderPauw sheet resistance monitor for this type resistor.

Specifics:

N+ Poly Silicide Blocked Resistor layer. Pad 10 provides backside substrate contact for backbias.

Res Group A: W=4um, Lsalblk=20um, Lend=0.7um, Num contacts/end=8.
Res Group B: W=1um, Lsalblk=5um, Lend=0.7um, Num contacts/end=2.
Res Group C: W=9um, Lsalblk=45um, Lend=0.7um, Num contacts/end=17.

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	VDP I+			18	VDP V+	
2	VDP I-			17	VDP V-	
3	Ra1d	W=4, Lsb=20, Lend=0.7, Nc=8		16	Ra3	
4	Ra2d			15	Ra4	
5	Rb1d	W=1, Lsb=5, Lend=0.7, Nc=2		14	Rb3	
6	Rb2d			13	Rb4	
7	Rc1d	W=9, Lsb=45. Lend=0.7, Nc=17		12	Rc3	
8	Rc2d			11	Rc4	
9	Res Com			10	Sub COM	

Diagram:

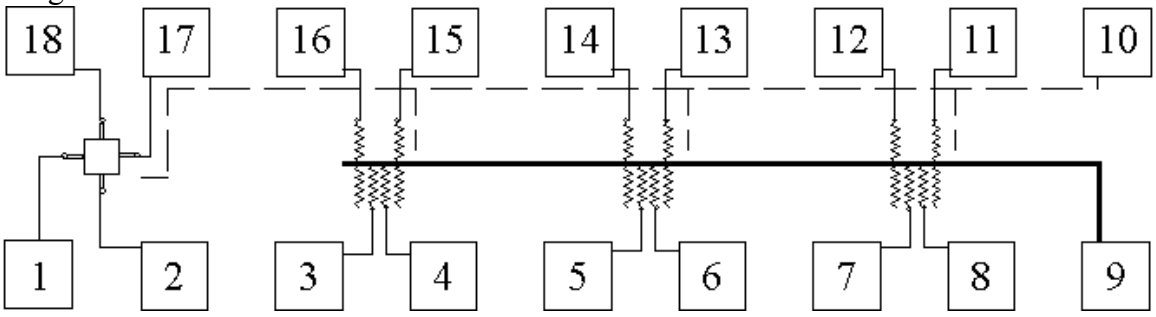


Figure 25, RmatP2NSB, N+ Poly Silicide Blocked

Location: B6 Name: RendP2NSB, N+ Poly Silicide Blocked

General Description:

This 18 pad module contains three 3-tap resistors, each having different widths. Resistors are of the same overall length and each tap on each resistor is in the same relative position on the resistors. Each of these resistors also have separate Current In (I+) terminals and share one Current Out (common I-) terminal. This module also contains a single-contact Kelvin-type test structure.

Specifics:

N+ Poly Silicide Blocked Resistor layer. Pad 10 provides backside substrate contact for backbias. Drawn contact size 0.22x0.22um.

3-Tap Res A: W=1um, L1=0.71um, L2=3.21um, L3=27.62um, Lend=0.7um, Ws=0.8um, Nc=2

3-Tap Res B: W=4um, L1=0.7um, L2=3.205um, L3=27.7um, Lend=0.7um, Ws=0.8um, Nc=8

3-Tap Res C: W=9um, L1=0.7um, L2=3.2um, L3=27.7um, Lend=0.7um, Ws=0.8um, Nc=17

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	Con I+	Single Kelvin Contact		18	Con V-	
2	Con V+			17	Con I-	
3	Ratap2	3-Tap Resistor A (1um)		16	Ratap3	
4	Ratap1			15	Ra I+	
5	Rbtap2	3-Tap Resistor B(4um)		14	Rbtap3	
6	Rbtap1			13	Rb I+	
7	Rctap2	3-Tap Resistor C(9um)		12	Rctap3	
8	Rctap1			11	Rc I+	
9	Res Com I-			10	Sub COM	

Diagram:

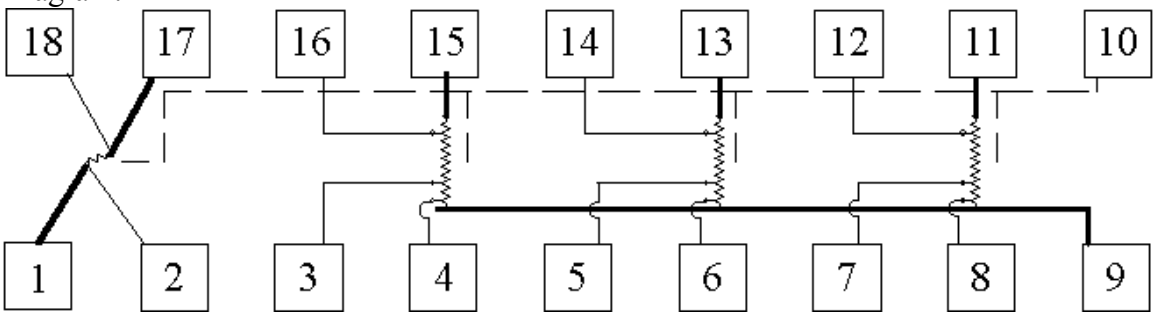


Figure 26, RendP2NSB, N+ Poly Silicide Blocked

Location: A7 Name: RmatP2PSB, P+ Poly Silicide Blocked

General Description:

This 18 pad module contains 3 sets of 4 matched resistors, each set representing one resistor width. Two of the resistors for each width are surrounded by 'dummy' resistors, the other two are not so protected. This module also contains a VanderPauw sheet resistance monitor for this type resistor.

Specifics:

P+ Poly Silicide Blocked Resistor layer. Pad 10 provides backside substrate contact for backbias.

Res Group A: W=4um, Lsalblk=20um, Lend=0.7um, Num contacts/end=8.
Res Group B: W=1um, Lsalblk=5um, Lend=0.7um~, Num contacts/end=2.
Res Group C: W=9um, Lsalblk=45um, Lend=0.7um, Num contacts/end=17.

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	VDP I+			18	VDP V+	
2	VDP I-			17	VDP V-	
3	Ra1d	W=4, Lsb=20, Lend=0.7, Nc=8		16	Ra3	
4	Ra2d			15	Ra4	
5	Rb1d	W=1, Lsb=5, Lend=0.7, Nc=2		14	Rb3	
6	Rb2d			13	Rb4	
7	Rc1d	W=9, Lsb=45. Lend=0.7, Nc=17		12	Rc3	
8	Rc2d			11	Rc4	
9	Res Com			10	Sub COM	

Diagram:

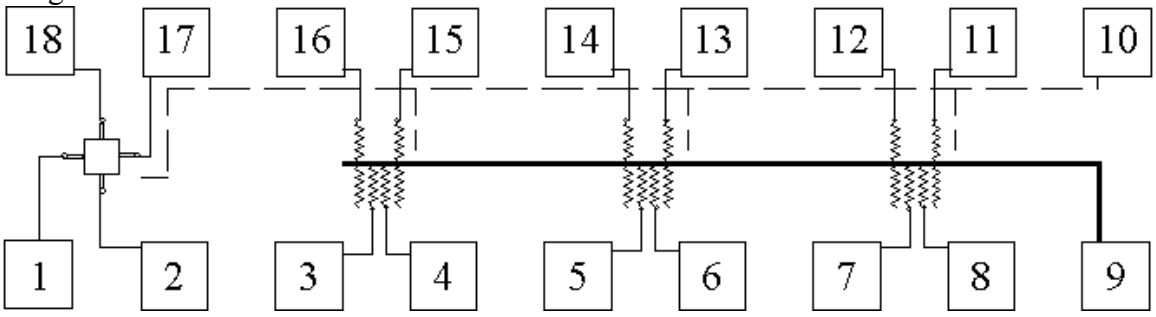


Figure 27, RmatP2PSB, P+ Poly Silicide Blocked

Location: B7 Name: RendP2PSB, P+ Poly Silicide Blocked

General Description:

This 18 pad module contains three 3-tap resistors, each having different widths. Resistors are of the same overall length and each tap on each resistor is in the same relative position on the resistors. Each of these resistors also have separate Current In (I+) terminals and share one Current Out (common I-) terminal. This module also contains a single-contact Kelvin-type test structure.

Specifics:

P+ Poly Silicide Blocked Resistor layer. Pad 10 provides backside substrate contact for backbias. Drawn contact size 0.22x0.22um.

3-Tap Res A: W=1um, L1=0.71um, L2=3.21um, L3=27.62um, Lend=0.7um, Ws=0.8um, Nc=2

3-Tap Res B: W=4um, L1=0.7um, L2=3.205um, L3=27.7um, Lend=0.7um, Ws=0.8um, Nc=8

3-Tap Res C: W=9um, L1=0.7um, L2=3.2um, L3=27.7um, Lend=0.7um, Ws=0.8um, Nc=17

Pad Assignments, Descriptions:

Pad #	Name	Description		Pad #	Name	
1	Con I+	Single Kelvin Contact		18	Con V-	
2	Con V+			17	Con I-	
3	Ratap2	3-Tap Resistor A (1um)		16	Ratap3	
4	Ratap1			15	Ra I+	
5	Rbtap2	3-Tap Resistor B(4um)		14	Rbtap3	
6	Rbtap1			13	Rb I+	
7	Rctap2	3-Tap Resistor C(9um)		12	Rctap3	
8	Rctap1			11	Rc I+	
9	Res Com I-			10	Sub COM	

Diagram:

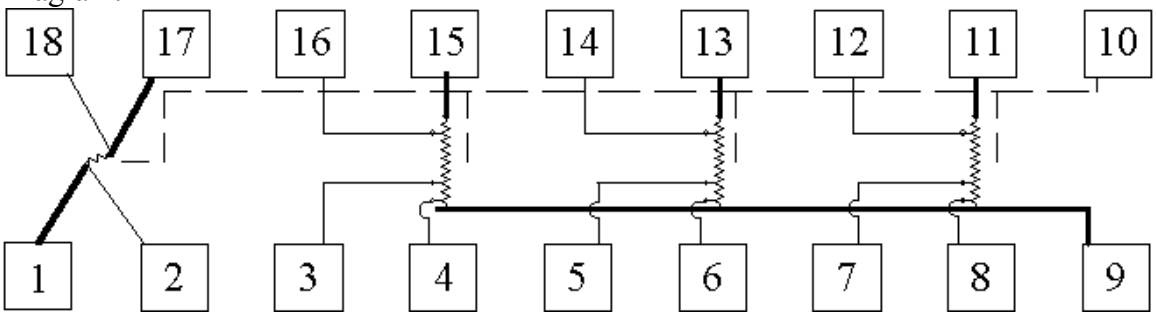
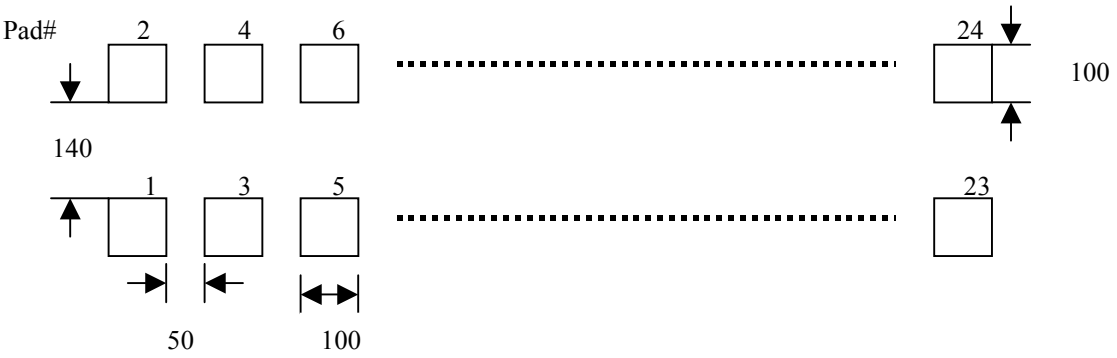


Figure 28, RendP2PSB, P+ Poly Silicide Blocked

V. Process benchmark

PAD RING

The pad ring used in these structures have following dimensions and spaces(unit: um) :



IMPORTANT NOTICE:

Metal 1 & 2 are used in most of structures for interconnect ion.

Module CS_RO_mod1

- **Module CS_RO_mod1 contains Ring Oscillators for model calibration.**
- **The ring oscillator contains 61 stages inverter chain with 4 kind of metal loading. The LPE structure for 4 kind of metal1 loading**
- **Metal3 is used for this Module.**

The operation of the oscillators(RO_INV1-RO_INV9) is as follows:

RNG_DLYN: High to force oscillation or "ringing".
Low to use the cell chain as a delay line.
OSC_IN: Input when in delay mode. Active high enable when in ring mode (Low will initialize the osc.).
OSC_OUT: Buffered Output of oscillator.

S/N	Structure	Wn / Wp (um)	L (um)	Remarks
1.	RO_023X023_GND	10/20	0.18	Thin gate 61-stage INV. With M1 loading. Signal line with neighboring ground line Metal1 Width:0.23um , Metal1 Space:0.23um. Metal Length: 700um
2.	RO_INV_N04P08_05	0.4/0.8	0.5	Thin gate 127-stage INV. No loading.

- Pads assignment

RO_INV_N04P08_05: VDD_CORE	**1**	**2**	RO_INV_N04P08_05: VSS_CORE
RO_INV_N04P08_05: VDD_BUFFER	**3**	**4**	RO_INV_N04P08_05: VSS_BUFFER
RO_023X023_GND :VSS	**21**	**22**	Not use
RO_023X023_GND:VDD	**23**	**24**	RO_023X023_GND:OUT

Module CS_RO_mod2

- **Module CS_RO_mod2 contains Ring oscillators .**

- Structures:

1. Ring Oscillators

S/N	Structure	Wn / Wp (um)	L (um)	Remarks
1.	TN-RO4-NOR	5/10	0.18	Thin gate 127-stage NOR gate RO. No loading
2.	TN-RO5-NAND	5/10	0.18	Thin gate 127-stage NAND gate RO. No loading.
3.	TN-RO6	10/20	0.18	Thin gate 127-stage INV RO , No loading.
4.	TN-RO7	10/20	0.18	Thin gate 127-stage INV RO with FO3
5.	TK-RO1	10/20	0.35	Thick gate 127-stage RO. No loading (4 pads)

- Pads assignment

MODULE05 BLOCK 2(Size x=390um, y=1880um)

TK RO1: GND	**1**	**2**	TK-RO1: VDD
TK-RO1: Enable	**3**	**4**	TK-RO1: OUT
TN-RO7: GND	**5**	**6**	TN-RO7: VDD
TN-RO7: Enable	**7**	**8**	TN-RO7: OUT
	9	**10**	
	11	**12**	
TN-RO4-NOR: GND	**13**	**14**	TN-RO4-NOR: VDD
TN-RO4-NOR: Enable	**15**	**16**	Not use
TN-RO5-NAND: GND	**17**	**18**	TN-RO5-NAND: VDD
TN-RO5-NAND: Enable	**19**	**20**	Not use
TN-RO6(INV Wn=10,Wp=20, L=0.18): GND	**21**	**22**	TN-RO6: VDD
TN-RO6: Enable	**23**	**24**	TN-RO5: OUT, TN-RO4-NOR: OUT, TN-RO5-NAND: OUT

Module CS_TKN/P_mod1/2

- **Module CS_TKN_mod1, CS_TKN_mod2, CS_TKP_mod1 and CS_TKP_mod2 contain thick gate NMOS and PMOS for DC, Temperature & Overlap Capacitance Spice modeling.**

- **Gate, drain ,source and bulk of all devices are isolated..**

L \ W	100	20	10	1.2	0.6	0.4	0.3
50							
20							
10			X			X, P	P
1.5			X				
0.8			X				
0.5			X				
0.36			X				
0.35			X	P		X, P	P
0.32			**X**				
0.30							
0.28							

1. X - Single Device with D, G, S, B isolated.
2. P - Parallel device (50x)
3. P* - Parallel device (40x)

Module CS_TKN_mod1

Description: Thick gate NMOS .
Purpose : IV/CV/Temperature modeling

- Pads assignment

Thick NMOS: W/L=10/10: Source	**1**	**2**	Thick NMOS: W/L=10/10:Body
Thick NMOS: W/L=10/10: Gate	**3**	**4**	Thick NMOS: W/L=10/10: Drain
Thick NMOS: W/L=10/0.35:Source	**5**	**6**	Thick NMOS: W/L=10/0.35:Body
Thick NMOS: W/L=10/0.35: Gate	**7**	**8**	Thick NMOS: W/L=10/0.35: Drain
Thick NMOS(50X): W/L=0.4/10: Source	**9**	**10**	Thick NMOS(50X): W/L=0.4/10:Body
Thick NMOS(50X): W/L=0.4/10: Gate	**11**	**12**	Thick NMOS(50X): W/L=0.4/10: Drain
Thick NMOS(50X): W/L=0.3/10: Source	**13**	**14**	Thick NMOS(50X): W/L=0.3/10:Body
Thick NMOS(50X): W/L=0.3/10: Gate	**15**	**16**	Thick NMOS(50X): W/L=0.3/10: Drain
Thick NMOS(50X): W/L=0.3/0.35: Source	**17**	**18**	Thick NMOS(50X): W/L=0.3/0.35:Body
Thick NMOS(50X): W/L=0.3/0.35: Gate	**20**	**21**	Thick NMOS(50X): W/L=0.3/0.35: Drain
Thick NMOS(50X):W/L=0.4/0.35:Source	**21**	**22**	Thick NMOS(50X): W/L=0.4/0.35:Body
Thick NMOS(50X): W/L=0.4/0.35: Gate	**23**	**24**	Thick NMOS(50X): W/L=0.4/0.35: Drain

Module CS_TKN_mod2

Description: Thick gate NMOS .
Purpose : IV/CV/Temperature modeling

- Pads assignment

Thick NMOS: W/L=10/1.5: Source	**1**	**2**	Thick NMOS: W/L=10/1.5:Body
Thick NMOS: W/L=10/1.5: Gate	**3**	**4**	Thick NMOS: W/L=10/1.5: Drain
Thick NMOS: W/L=10/0.8:Source	**5**	**6**	Thick NMOS: W/L=10/0.8:Body
Thick NMOS: W/L=10/0.8: Gate	**7**	**8**	Thick NMOS: W/L=10/0.8: Drain
Thick NMOS: W/L=10/0.5: Source	**9**	**10**	Thick NMOS: W/L=10/0.5:Body
Thick NMOS: W/L=10/0.5: Gate	**11**	**12**	Thick NMOS: W/L=10/0.5: Drain
Thick NMOS(50X):W/L=1.2/0.35:Source	**13**	**14**	Thick NMOS(50X): W/L=1.2/0.35:Body
Thick NMOS(50X): W/L=1.2/0.35: Gate	**15**	**16**	Thick NMOS(50X): W/L=1.2/0.35: Drain
Thick NMOS: W/L=10/0.32: Source	**17**	**18**	Thick NMOS: W/L=10/0.32:Body
Thick NMOS: W/L=10/0.32: Gate	**19**	**20**	Thick NMOS: W/L=10/0.32: Drain
Thick NMOS: W/L=10/0.36: Source	**21**	**22**	Thick NMOS: W/L=10/0.36:Body
Thick NMOS: W/L=10/0.36: Gate	**23**	**24**	Thick NMOS: W/L=10/0.36: Drain

Module CS_TKP_mod1

Description: Thick gate PMOS .
Purpose : IV/CV/Temperature modeling

- Pads assignment

Thick PMOS(50X): W/L=0.3/10: Source	**1**	**2**	Thick PMOS(50X): W/L=0.3/10:Body
Thick PMOS(50X): W/L=0.3/10: Gate	**3**	**4**	Thick PMOS(50X): W/L=0.3/10: Drain
Thick PMOS(50X): W/L=0.3/0.35: Source	**5**	**6**	Thick PMOS(50X): W/L=0.3/0.35:Body
Thick PMOS(50X): W/L=0.3/0.35: Gate	**7**	**8**	Thick PMOS(50X): W/L=0.3/0.35: Drain
Thick PMOS: W/L=10/10: Source	**9**	**10**	Thick PMOS: W/L=10/10:Body
Thick PMOS: W/L=10/10: Gate	**11**	**12**	Thick PMOS: W/L=10/10: Drain
Thick PMOS: W/L=10/0.35:Source	**13**	**14**	Thick PMOS: W/L=10/0.35:Body
Thick PMOS: W/L=10/0.35: Gate	**15**	**16**	Thick PMOS: W/L=10/0.35: Drain
Thick PMOS(50X): W/L=0.4/10: Source	**17**	**18**	Thick PMOS(50X): W/L=0.4/10:Body
Thick PMOS(50X): W/L=0.4/10: Gate	**19**	**20**	Thick PMOS(50X): W/L=0.4/10: Drain
Thick PMOS(50X):W/L=0.4/0.35:Source	**21**	**22**	Thick PMOS(50X): W/L=0.4/0.35:Body
Thick PMOS(50X): W/L=0.4/0.35: Gate	**23**	**24**	Thick PMOS(50X): W/L=0.4/0.35: Drain

Module CS_TKP_mod2

Description: Thick gate PMOS .
Purpose: IV/CV/Temperature modeling

- Pads assignment

Thick PMOS: W/L=10/1.5: Source	**1**	**2**	Thick PMOS: W/L=10/1.5:Body
Thick PMOS: W/L=10/1.5: Gate	**3**	**4**	Thick PMOS: W/L=10/1.5: Drain
Thick PMOS: W/L=10/0.8:Source	**5**	**6**	Thick PMOS: W/L=10/0.8:Body
Thick PMOS: W/L=10/0.8: Gate	**7**	**8**	Thick PMOS: W/L=10/0.8: Drain
Thick PMOS: W/L=10/0.5: Source	**9**	**10**	Thick PMOS: W/L=10/0.5:Body
Thick PMOS: W/L=10/0.5: Gate	**11**	**12**	Thick PMOS: W/L=10/0.5: Drain
Thick PMOS(50X):W/L=1.2/0.35:Source	**13**	**14**	Thick PMOS(50X): W/L=1.2/0.35:Body
Thick PMOS(50X): W/L=1.2/0.35: Gate	**15**	**16**	Thick PMOS(50X): W/L=1.2/0.35: Drain
Thick PMOS: W/L=10/0.32: Source	**17**	**18**	Thick PMOS: W/L=10/0.32:Body
Thick PMOS: W/L=10/0.32: Gate	**19**	**20**	Thick PMOS: W/L=10/0.32: Drain
Thick PMOS: W/L=10/0.36: Source	**21**	**22**	Thick PMOS: W/L=10/0.36:Body
Thick PMOS: W/L=10/0.36: Gate	**23**	**24**	Thick PMOS: W/L=10/0.36: Drain

Module CS_TN/P_mod1/2

- **Module CS_TN_mod1 and CS_TN_mod2 and CS_TP_mod1 and CS_TP_mod2 contain thin gate NMOS and PMOS for DC, Temperature & Overlap Capacitance Spice modeling.**
- **Gate, drain, source and bulk of all devices are isolated..**

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L \ W	100	20	10	1.6	0.8	0.44	0.22	0.2
50								
20								
10			X			P	X, P	
1.2			X					
0.5			X					
0.22			X					
0.18			X, P	P	X, P	P	X, P	
0.16			X					

1. X - Single Device with D, G, S, B isolated.
2. P - Parallel device (50x)
3. P* - Parallel device (20x)

Module CS_TN_mod1

Description: Thin gate NMOS .
Purpose : IV/CV/Temperature modeling

- Pads assignment

Thin NMOS(50X):W/L=0.8/0.18:Source	**1**	**2**	Thin NMOS(50X): W/L=0.8/0.18:Body
Thin NMOS(50X): W/L=0.8/0.18: Gate	**3**	**4**	Thin NMOS(50X): W/L=0.8/0.18: Drain
Thin NMOS(50X): W/L=0.44/10: Source	**5**	**6**	Thin NMOS(50X): W/L=0.44/10:Body
Thin NMOS(50X): W/L=0.44/10: Gate	**7**	**8**	Thin NMOS(50X): W/L=0.44/10: Drain
Thin NMOS: W/L=10/10: Source	**9**	**10**	Thin NMOS: W/L=10/10:Body
Thin NMOS: W/L=10/10: Gate	**11**	**12**	Thick NMOS: W/L=10/10: Drain
Thin NMOS: W/L=10/0.18:Source	**13**	**14**	Thin NMOS: W/L=10/0.18:Body
Thin NMOS: W/L=10/0.18: Gate	**15**	**16**	Thin NMOS: W/L=10/0.18: Drain
Thin NMOS(50X): W/L=0.22/10: Source	**17**	**18**	Thin NMOS(50X): W/L=0.22/10:Body
Thin NMOS(50X): W/L=0.22/10: Gate	**19**	**20**	Thin NMOS(50X): W/L=0.22/10: Drain
Thin NMOS(50X):W/L=0.22/0.18:Source	**21**	**22**	Thin NMOS(50X): W/L=0.22/0.18:Body
Thin NMOS(50X): W/L=0.22/0.18: Gate	**23**	**24**	Thin NMOS(50X): W/L=0.22/0.18: Drain

Module CS_TN_mod2

Description: Thin gate NMOS .
Purpose : IV/CV/Temperature modeling

- Pads assignment

Thin NMOS: W/L=10/1.2: Source	**1**	**2**	Thin NMOS: W/L=10/1.2:Body
Thin NMOS: W/L=10/1.2: Gate	**3**	**4**	Thin NMOS: W/L=10/1.2: Drain
Thin NMOS: W/L=10/0.5:Source	**5**	**6**	Thin NMOS: W/L=10/0.5:Body
Thin NMOS: W/L=10/0.5: Gate	**7**	**8**	Thin NMOS: W/L=10/0.5: Drain
Thin NMOS: W/L=10/0.22: Source	**9**	**10**	Thin NMOS: W/L=10/0.22:Body
Thin NMOS: W/L=10/0.22: Gate	**11**	**12**	Thin NMOS: W/L=10/0.22: Drain
Thin NMOS(50X):W/L=1.6/0.18:Source	**13**	**14**	Thin NMOS(50X): W/L=1.6/0.18:Body
Thin NMOS(50X): W/L=1.6/0.18: Gate	**15**	**16**	Thin NMOS(50X): W/L=1.6/0.18: Drain
Thin NMOS(50X):W/L=0.44/0.18:Source	**17**	**18**	Thin NMOS(50X): W/L=0.44/0.18:Body
Thin NMOS(50X): W/L=0.44/0.18: Gate	**19**	**20**	Thin NMOS(50X): W/L=0.44/0.18: Drain
Thin NMOS: W/L=10/0.16:Source	**21**	**22**	Thin NMOS: W/L=10/0.16:Body
Thin NMOS: W/L=10/0.16: Gate	**23**	**24**	Thin NMOS: W/L=10/0.16: Drain

Module CS_TP_mod1

Description: Thin gate PMOS .
Purpose : IV/CV/Temperature modeling

- Pads assignment

Thin PMOS(50X):W/L=0.8/0.18:Source	**1**	**2**	Thin PMOS(50X): W/L=0.8/0.18:Body
Thin PMOS(50X): W/L=0.8/0.18: Gate	**3**	**4**	Thin PMOS(50X): W/L=0.8/0.18: Drain
Thin PMOS(50X): W/L=0.44/10: Source	**5**	**6**	Thin PMOS(50X): W/L=0.44/10:Body
Thin PMOS(50X): W/L=0.44/10: Gate	**7**	**8**	Thin PMOS(50X): W/L=0.44/10: Drain
Thin PMOS: W/L=10/10: Source	**9**	**10**	Thin PMOS: W/L=10/10:Body
Thin PMOS: W/L=10/10: Gate	**11**	**12**	ThickPNMOS: W/L=10/10: Drain
Thin PMOS: W/L=10/0.18:Source	**13**	**14**	Thin PMOS: W/L=10/0.18:Body
Thin PMOS: W/L=10/0.18: Gate	**15**	**16**	Thin PMOS: W/L=10/0.18: Drain
Thin PMOS(50X): W/L=0.22/10: Source	**17**	**18**	Thin PMOS(50X): W/L=0.22/10:Body
Thin PMOS(50X): W/L=0.22/10: Gate	**19**	**20**	Thin PMOS(50X): W/L=0.22/10: Drain
Thin PMOS(50X):W/L=0.22/0.18:Source	**21**	**22**	Thin PMOS(50X): W/L=0.22/0.18:Body
Thin PMOS(50X): W/L=0.22/0.18: Gate	**23**	**24**	Thin PMOS(50X): W/L=0.22/0.18: Drain

Module CS_TP_mod2

Description: Thin gate PMOS .
Purpose : IV/CV/Temperature modeling

- Pads assignment

Thin PMOS: W/L=10/1.2: Source	**1**	**2**	Thin PMOS: W/L=10/1.2:Body
Thin PMOS: W/L=10/1.2: Gate	**3**	**4**	Thin PMOS: W/L=10/1.2: Drain
Thin PMOS: W/L=10/0.5:Source	**5**	**6**	Thin PMOS: W/L=10/0.5:Body
Thin PMOS: W/L=10/0.5: Gate	**7**	**8**	Thin PMOS: W/L=10/0.5: Drain
Thin PMOS: W/L=10/0.22: Source	**9**	**10**	Thin PMOS: W/L=10/0.22:Body
Thin PMOS: W/L=10/0.22: Gate	**11**	**12**	Thin PMOS: W/L=10/0.22: Drain
Thin PMOS(50X):W/L=1.6/0.18:Source	**13**	**14**	Thin PMOS(50X): W/L=1.6/0.18:Body
Thin PMOS(50X): W/L=1.6/0.18: Gate	**15**	**16**	Thin PMOS(50X): W/L=1.6/0.18: Drain
Thin PMOS(50X):W/L=0.44/0.18:Source	**17**	**18**	Thin PMOS(50X): W/L=0.44/0.18:Body
Thin PMOS(50X): W/L=0.44/0.18: Gate	**19**	**20**	Thin PMOS(50X): W/L=0.44/0.18: Drain
Thin PMOS:W/L=10/0.16:Source	**21**	**22**	Thin PMOS: W/L=10/0.16:Body
Thin PMOS: W/L=10/0.16: Gate	**23**	**24**	Thin PMOS: W/L=10/0.16: Drain