This document contains pages from the PCM Engineering Binder.

PCM stands for Process Control Monitor. This may be called WAT (Wafer Acceptance Testing) or ETEST (Electrical Test) at other companies.

These pages show a very early stage of evolution of the system used at this unnamed company. In particular more advanced databasing, information sharing over the web, and data analysis reports evolved.

Currently most Fabless IC companies accept this type of data unverified from the silicon foundries using a "lean manufacturing" rationale to justify this decision. Data is imported directly over the Web from the foundaries.

Fred E Wahl, 6/18/2004

PCM Engineering

Introduction

PCM stands for Process Control Monitor. In integrated circuit manufacturing it is used to mean two different but related things. The first meaning is as a generic name for an activity whose purpose is to monitor and control by statistical means the quality of silicon processing used to fabricate the required semiconductor wafers. This activity usually includes the design of specialized electrical test structures and chips, the automated DC electrical testing of these test chips, and the statistical analysis and interpretation of the resulting process parameter data. The second meaning of PCM applies more specifically to the test chip (in its various forms) used by this activitv.

In order to successfully perform this PCM function, has organized this activity into separate functional groups. The Operations group provides test operators to perform the day-to-day wafer testing. The Maintenance group provides the technicians needed to set-up the tester and debug system problems. A PCM Engineering group provides the remaining resource to develop the test chips, test system, test programs and procedures, the data base and analysis software, and to provide the reports. The Process Engineering group receives these reports and works with the wafer Fab to correct any processing problems detected.

This binder serves to document the PCM system from an engineering point of view. It does not contain all PCM documents but does attempt to contain at least one example of each type of document needed to understand and modify the system. Separate binders provide information specific to particular wafer fabs, PCM system program source codes and complete sets of Setup documents.

PCM Usage Philosopy

(I is a manufacturer of integrated circuits which contracts independent wafer manufacturing fabs to process the silicon wafers which are used to realize its custom logic chip designs. In order to control wafer quality each contracting fab performs DC electrical testing on special silicon test structures on its wafers. These special test structures may be located on a small portion of the circuit die ("drop-ins"), they may be placed on their own specialized chip ("PCM test chip"), or they may be placed between the rows and columns of the actual product chip ("Scribe Lane Modules"). Data collected from these PCM (Process Control Monitor) devices is used in SPC (Statistical Process Control) methods to monitor and control the wafer manufacturing process.

• What the Fabs do

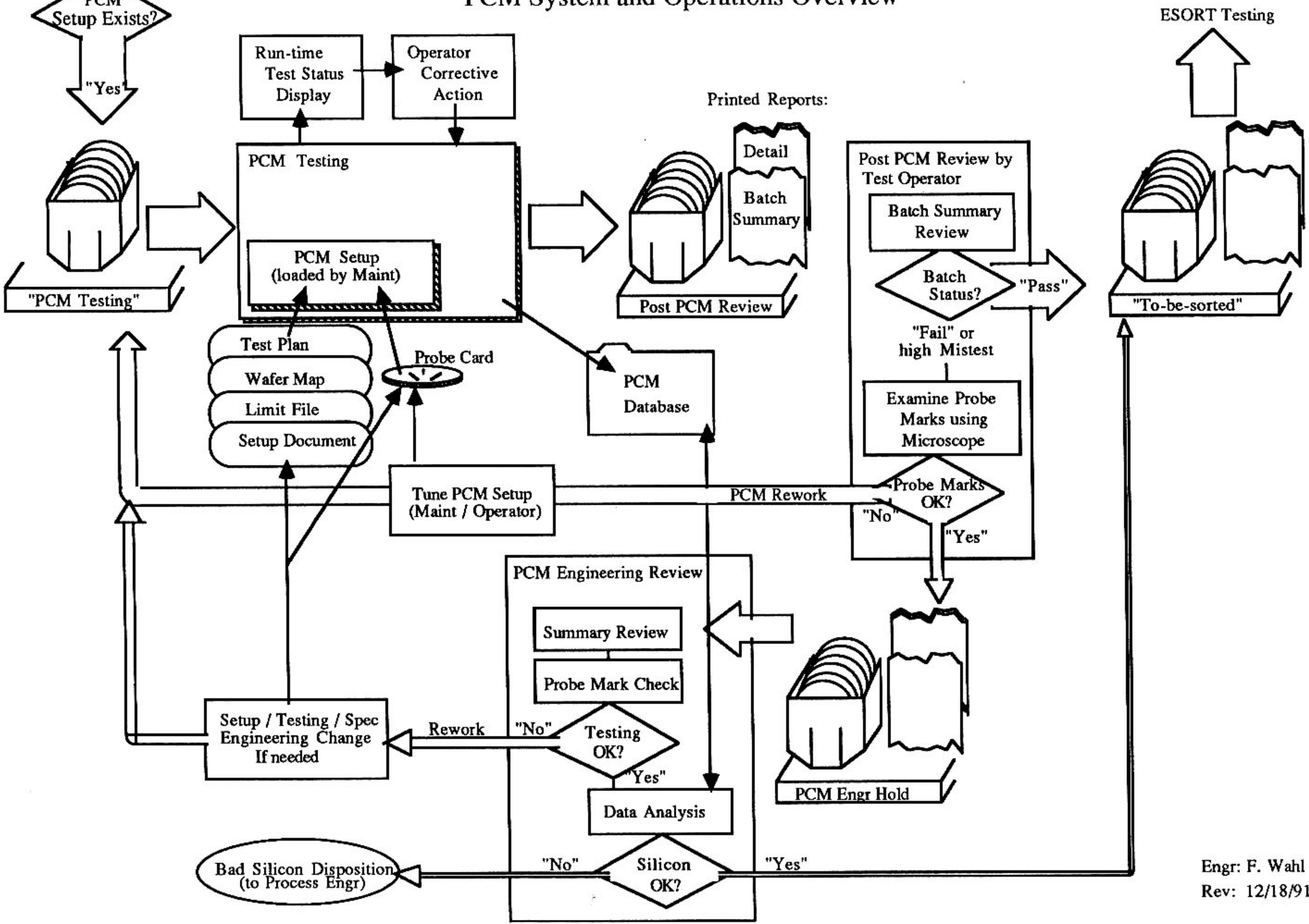
Per contractual agreements (requires each fab to perform 100% wafer testing and provide data proving that its wafers meet our DC electrical specifications. They are expected to use valid SPC methods internally, but to a certain extent each fab is considered to be a wafer manufacturing "black box".

• What Cirrus does to monitor wafer quality

(performs its own PCM test and SPC monitoring activity to mirror that performed by each fab. We monitor parameters which correspond to the negotiated specifications and additional parameters which help us to understand product yield and performance. In this way we can double check what the fab tells us about the wafers. By using the test data on incomming wafers we provide a "first line of defense" to gaurd against defects in our product quality.

• Other Uses for PCM at (

PCM also plays a strong role in engineering understanding of new process qualification and new product qualification. Non production specialized PCMs chips, testing and analysis is done by Process and Device physicists to qualify each new process at each wafer fab contractor. Special characterization is done on existing processes using our PCM test ability in order to explore regions of device behavior needed by unusual circuits such as low voltage or power battery operated chips.


PCM System and Operations Overview
ESORT "In-Processing"
PCM Setup Exists?
"Yes"
"PCM Testing"
Run-time Test Status Display
Operator Corrective Action
PCM Testing
PCM Setup (loaded by Maint)
Test Plan
Wafer Map
Limit File
Setup Document
Probe Card
Tune PCM Setup (Maint / Operator)
Printed Reports:
Detail
Batch Summary
Post PCM Review
PCM Database
PCM Rework
Post PCM Review by Test Operator
Batch Summary Review
Batch Status?
"Pass"
"Fail" or high Mistest
Examine Probe Marks using Microscope
Probe Marks OK?
"No"
"Yes"
ESORT Testing
"To-be-sorted"
PCM Engr Hold
PCM Engineering Review
Summary Review
Probe Mark Check
Testing OK?
"No"
"Yes"
Rework
Setup / Testing / Spec Engineering Change If needed
Data Analysis
Silicon OK?
"No"
"Yes"
Bad Silicon Disposition (to Process Engr)
Engr: F. Wahl
Rev: 12/18/91

PCM Engineering

Operations Role Overview

Test operations supervisors determine product testing schedules, request Maintenance to install the proper product PCM test setup if it exists, and communicate the need for a new PCM test setup if it does not exist to PCM Engineering. Test operations provides the personnel who are the PCM test operators.

1) Operations is responsible for maintaining wafer "shelves" where material worked on is staged. These include a "PCM testing" shelf, a "Post PCM Review" staging area, a "PCM Engr hold" shelf and an "ESORT to-be-sorted" shelf.

2) Test operators are required to understand the "Run time Test Status Display" and use the corrective action procedures. They are expected to minimize "Red" flags (mistest indicators) during testing. If this is done little PCM rework should be required.

3) Test operators perform the PCM testing on wafers from the "PCM testing" shelf and subsequently move the wafers and the resulting printed test results reports (Detail and Batch Summary) to the "Post PCM review" station. Here the operator reviews the Batch Summary for correct testing. If the Batch Summary indicates that the batch is a PASS and no high mistest warnings are printed on the Batch summary, then the operator transfers the lot and its printed reports to the "ESORT to-be-sorted" shelf. If the Batch summary indicates FAIL or if a high mistest warning is printed the operator checks the tested wafers under the microscope for proper probe marks. If necessary the lot is reworked by the operator. The operator may call upon Maintenance to assist with tester problem correction before the rework is performed. If in the operators best judgement a FAIL or high-mistest flagged lot is not an operational problem, then the operator transfers the lot to the "PCM engr Hold" shelf for Engr examination of the problem.

4) Test operators may be requested to perform PCM test rework if PCM Engineering determines that wafers transferred to the "PCM engr hold" shelf are mistested. Engr will annotate the Batch Summary requesting PCM testing rework and place the lot and reports back on the "PCM testing" shelf. Upon rework the old Batch Summary and Detail report are discarded unless otherwise notified.

PCM Engineering

Maintenance Role Overview

Maintenance provides service to Operations and PCM Engineering to help gaurantee the success of the PCM function. It provides:

1) Upon request by Test Operations, maintenance produces PCM tester setups. Maintenance delivers to Operations a PCM tester ready to test a specific product wafer. They load the Test Program, Probe card and check that the system successfully tests the requested product. To do this they must be able to read and understand PCM Test Setup documents produced by Engr. Maintenance understands the "Run-time Test Status Display" meaning and usage and is able to interpret signs of proper testing on the PCM Batch Summary.

2) When test operators have difficulty with the tester, they provide Setup tuning of probe card, pin alignment and initial system diagnostics. If problem is beyond their expertise they call in PCM Engineering.

3) Maintenance provides a PCM probe card inventory and repair scheduling service. Probe card designs provided by Eng are communicated to the probe card manufacturer. Maintenance assists with the testing and qualification of received probe cards.

4) Maintenance assists Engr to Diagnose and Repair tester and prober problems. A weekly tester diagnostic is run and tester UP/DOWN status is flagged. A log of PMs and Diagnostic checks is maintained. Maintenance assists Engr to assure that tester calibrations are performed on time.

5) Maintenance powers the system up and down when needed due to planned or unplanned power outages. They use the proper power up/down procedures to protect against data loss.

6) Where consumable supplies have been determined, maintenance provides for the stocking and reinventory of items such as printer paper and ink.

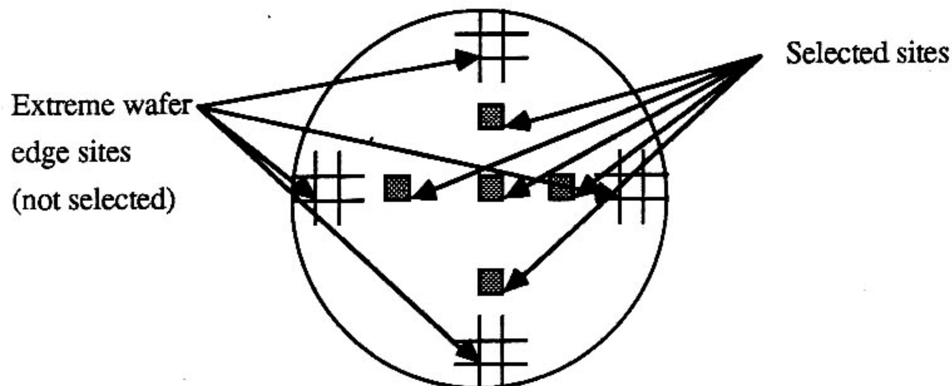
PCM Sampling Plan

Internally (I performs what is known as sampled wafer PCM testing on all production wafer lots. Every fifth wafer is tested. So in the case of a 25 wafer lot 5 wafers would be PCM tested.

On wafers selected for testing either 3 or 5 PCM sites are examined, depending upon the availability of test structures. If sufficient structures exist five well-spaced sites are used.

Sites are selected during PCM Wafer Map creation and are chosen to sample wafer parameter variation accurately. Guidelines for chosing the 5 sites are as follows:

1) Chose one site near the center of the wafer.
2) Chose others near the wafer edges: left , right, top & bottom
3) Move in one possible site from the extreme wafer edges.



The PCM at each site may be of one of three forms: 1) separate PCM test chip
2) drop-in test structures
or 3) scribe lane modules

To determine the actual site sampling one must refer to the PCM Setup Document for the particular product.

New Products, also known as Prototype Lots are tested on a 100% wafer sampling plan until revisioned, qualified for production, or until the first 10 lots have been fabbed and tested, whichever comes first.

PCM TEST SET-UP
For
I0149AA -- 6 " ZIGGY (Fab E)

Rev: 10/28/91
Fred Wahl

PROBER SETUP AND PROCEDURES:

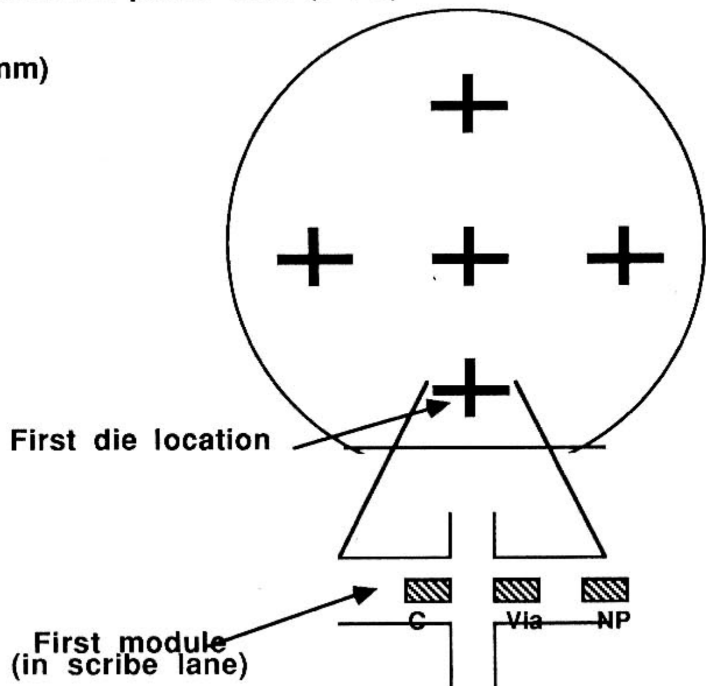
PROBE CARD: Use "Cirrus scribe lane #1" standard probe card (3-4-3)

WAFER SIZE: 6" (set wafer diameter to 150mm)
DIE SIZE: x=7.06mm y=6.45mm
FLAT: 0

1. Position prober to first die and module.
2. Set first die and autoprobe.

TEST PROCEDURE:

1. Use testplan and map D if in Engineering mode. (tests C, NP and Via)
2. Enter lot number.
3. Achieve no red flags on initial setup and minimum red flags during testing.



Calculation of CP/CPK's for PCM data

Fred Wahl
2/12/92

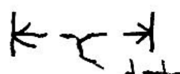
from a "LIMIT FILE"

```
*-----------------------------------------------------------------------*
'*(      L      ETest Limit File:    LIM_B_A    rev: 02/05/92.0 engr: FEW
 *Technology     Wafer_Fab     Test_plan
    C12              B             A
'wafer_pass=1/1 2/2 2/3 3/4 3/5 66.0% good die per die tested per wafer.
'Batch_pass=1/1 2/2 2/3 3/4 4/5 80.0% good waf per waf tested per batch.
'*Test Limits:
'*                        Valid      USL        LSL        Valid         TAR
'*   Test                 Testing    Spec       Spec       Testing
'$   Name         Use     Max        Max        Min        Min         Target     Units
'1   VTSATN_1.2   S       2.0        1.15       0.55       0.0          0.80      volts
'2   BETA_N       S       2.E-3      6.5E-4     2.5E-4     1.E-5        4.5E-4    mhos/.
'3   IDSATN       A       0.1        2.6E-3     0.9E-3     1.E-5        1.9E-3    amps
'4   LEAKN        A       1.E-1      8.E-6      -5.E-9     -1.E-3      <2.E-7     amps
'5   BVDSSN       A       30.0       25.0       6.00       -0.1        >7.00      volts
 •
 •
```

Limit type controlled by > or < sign in front of target

double-sided (VTSATN_1.2, BETA_N, IDSATN)

single-sided (LEAKN, BVDSSN)



data is sorted and is kept if it is between these limits for both double and single-sided limits. → a mean (A4) and standard deviation (SIGMA) are calculated for the sorted data

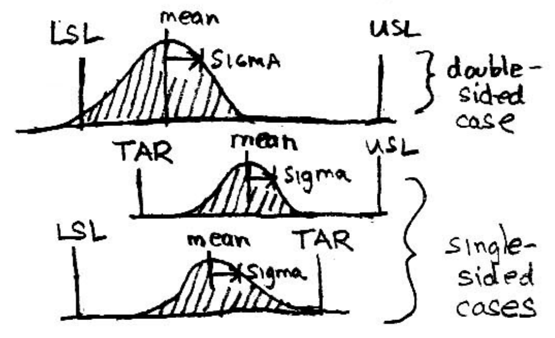
CP/CPK are then calculated using this BASIC language code

from custom program "dBASE"

```
 •
 •
Cp=0
IF Sigma>0 THEN
   Cp=(Usl-Lsl)/(6.0*Sigma)
   IF Limits(A,6)<0 THEN Cp=(Tar-Lsl)/(6.0*Sigma)
   IF Limits(A,6)>0 THEN Cp=(Usl-Tar)/(6.0*Sigma)
END IF
Cpk=0
Cpk1=0
Cpk2=0

IF Limits(A,6)=0 THEN    ! double sided limits
  IF Sigma>0 THEN Cpk1=(A4-Lsl)/(3*Sigma)
  IF Sigma>0 THEN Cpk2=(Usl-A4)/(3*Sigma)
  Cpk=MIN(Cpk1,Cpk2)
END IF
IF Limits(A,6)>0 THEN    ! data greater than target
  IF Sigma>0 THEN Cpk=(A4-Tar)/(3*Sigma)
END IF
IF Limits(A,6)<0 THEN    ! data less than target
  IF Sigma>0 THEN Cpk=(Tar-A4)/(3*Sigma)
END IF
 •
 •
```

(variable Limits(A,6) tells program what type of limit is being used)



Finally a report is printed

from resulting "STATISTICS REPORT"

Fab B C12 Process Jan 1992 (All Lots less those damaged by testing)
Electrical Parameter STATISTICS Report
Wafer Fab B
Test Plan A
1 Jan 1992 to 31 Jan 1992

PARAMETER	AVERAGE	SIGMA	Cp	Cpk	TARGET
VTSATN_1.2	+8.82E-01	+4.68E-02	+2.14E+00	[illegible]	+8.00E-01
BETA_N	+4.35E-04	+3.86E-05	+1.73E+00	+1.60E+00	+4.50E-04
IDSATN	+1.74E-03	+1.02E-04	+2.77E+00	+2.73E+00	+1.80E-03
LEAKN	+1.51E-09	+1.99E-08	+1.72E+00	+3.32E+00	+2.00E-07
BVDSSN	+1.39E+01	+1.49E+00	[illegible]	+1.54E+00	+7.00E+00

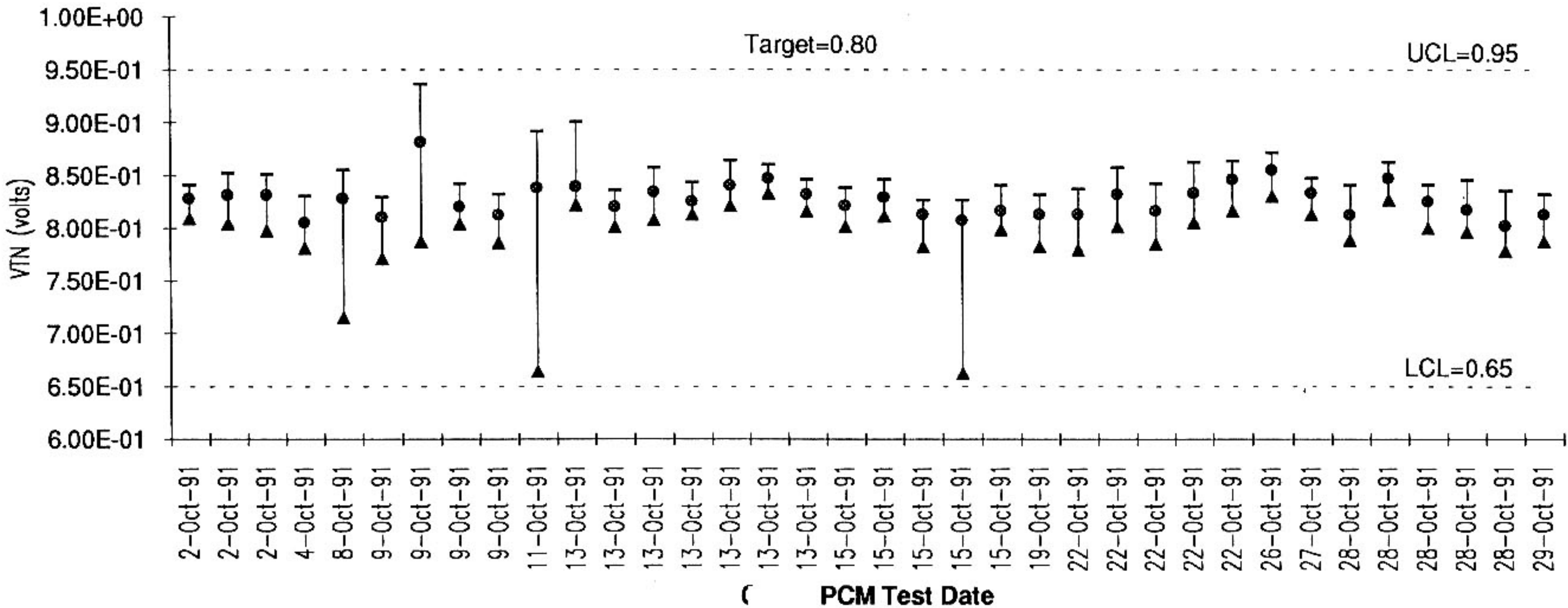
•
•

```
1    !*-----------------------------------------------------------------------------*
2    !*(     |     ETest Limit File:   LIM_E_D   rev: 10/20/91.0  engr: FEW
3    !*Technology    Wafer_Fab    Test_plan
4    !  C12              E              D
5    !Wafer_pass=1/1 2/2 2/3 3/4 3/5 66.0% good die per die tested per wafer.
6    !Batch_pass=1/1 2/2 2/3 3/4 4/5 80.0% good waf per waf tested per batch.
7    !*Test Limits:
8    !*                 Valid                           Valid
10   !*   Test          Testing    Spec      Spec       Testing
11   !#   Name     Use  Max        Max       Min        Min        Target     Units
21   !1  C10_M1-M1  A   1.E-3      5.E-6     -5.E-9     -1.E-6     1.E-10     amps
31   !2  C10_M2-M2  A   1.E-3      5.E-9     -5.E-9     -1.E-6     1.E-10     amps
41   !3  C12_M1-M1  A   1.E-3      5.E-6     -5.E-9     -1.E-6     1.E-10     amps
51   !4  C12_M2-M2  A   1.E-3      1.E-5     -5.E-9     -1.E-6     1.E-10     amps
61   !5  C10_M1-CON A   1.E+4      300.0     50.0       1.0        150.0      ohms
62   !6  C10_M2-CON A   1.E+4      300.0     10.0       1.0        50.0       ohms
63   !7  C12_M1-CON A   1.E+4      400.0     100.0      1.0        180.0      ohms
64   !8  C12_M2-CON A   1.E+4      600.0     20.0       1.0        100.0      ohms
65   !9  VTSN_1.2D  S   2.0        0.95      0.65       0.0        0.80       volts
66   !10 BTN_1.2    S   4.E-3      2.E-3     1.1E-3     5.E-4      1.3E-3     mhos/v
67   !11 IDSN_1.2   A   0.1        6.E-3     2.E-3      1.E-6      4.0E-3     amps
68   !12 LEAKN_1.2  A   0.1        2.E-4     -5.E-9     -1.E-3     2.E-6      amps
69   !13 VTSN_1.6   A   2.0        1.2       0.5        0.0        0.80       volts
70   !14 BTN_1.6    A   1.E-2      2.E-3     4.E-4      1.E-6      9.E-4      mhos/v
71   !15 IDSN_1.6   A   0.1        6.E-3     3.E-3      1.E-6      4.E-3      amps
72   !16 LEAKN_1.6  A   0.1        1.E-4     -5.E-9     -1.E-3     1.E-6      amps
73   !17 VTSN_20    A   2.0        1.5       0.4        0.0        0.95       volts
74   !18 BTN_20     A   1.E-3      5.E-4     4.E-5      1.E-7      7.6E-5     mhos/v
75   !19 IDSN_20    A   0.1        5.0E-4    4.0E-4     1.E-7      4.5E-4     amps
76   !20 LEAKN_20   A   0.1        1.E-6     -5.E-9     -1.E-3     5.E-9      amps
77   !21 VTSP_1.2   S   0.0        -0.65     -0.95      -2.0       -0.80      volts
78   !22 BTP_1.2    S   1.E-3      5.9E-4    3.5E-4     1.E-4      6.E-4      mhos/v
79   !23 IDSP_1.2   A   -1.E-6     -1.0E-3   -3.5E-3    -0.1       -3.E-3     amps
80   !24 LEAKP_1.2  A   1.E-3      5.E-9     -5.E-7     -0.1       -5.E-9     amps
81   !25 VTSP_1.6   A   0.0        -0.35     -1.2       -2.0       -0.85      volts
82   !26 BTP_1.6    A   1.E-2      1.6E-3    1.E-4      1.E-6      4.5E-4     mhos/v
83   !27 IDSP_1.6   A   -1.E-6     -1.75E-3  -2.25E-3   -0.1       -2.E-3     amps
84   !28 LEAKP_1.6  A   1.E-3      5.E-9     -5.E-10    -0.1       -1.E-10    amps
85   !29 VTSP_20    A   0.0        -0.2      -2.0       -2.0       -0.98      volts
86   !30 BTP_20     A   1.E-2      1.2E-4    1.E-5      1.E-6      2.3E-5     mhos/v
87   !31 IDSP_20    A   -1.E-6     -1.E-4    -1.6E-4    -0.10      -1.3E-4    amps
88   !32 LEAKP_20   A   1.E-3      5.E-9     -1.E-9     -0.1       -1.5E-10   amps
89   !33 P+CONTACTS A   1.E+5      1.E+4     2.E+3      1.0        7.E+3      ohms
90   !34 N+CONTACTS A   1.E+4      1.5E+4    700.0      1.0        1.5E+3     ohms
91   !35 POLY_CTS   A   5.E+4      1.2E+4    1.E+3      1.0        1.8E+3     ohms
92   !36 100x100_PR A   1.E+4      800.0     10.0       1.0        35.0       ohms
93   !37 2x100_PR   A   1.E+4      980.0     720.0      1.0        820.0      ohms
94   !38 VIA_R      A   1.E+4      1.5E+3    30.0       1.0        80.0       ohms
95   !39 GATE_CAP   A   1.E-11     4.E-12    8.E-13     1.E-13     2.3E-12    farad
97   1234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234
```

File: "/basic/FAB_E/TEST_PLAND"

FAB_E
C12
Testplan D

```
10   ! <MODULE> 1
20   ! BRIDGE      C10_M1-M1            :N  C10        22,20
30   ! BRIDGE      C10_M2-M2            :N  C10        17,20
40   ! BRIDGE      C12_M1-M1            :N  C10        11,9
50   ! BRIDGE      C12_M2-M2            :N  C10        11,15
60   ! RESZP       C10_M1-CONT.         :N  C10        22,21
70   ! RESZP       C10_M2-CONT.         :N. C10        17,16
80   ! RESZP       C12_M1-CONT.         :N  C10        10,9
90   ! RESZP       C12_M2-CONT.         :N  C10        15,14
91   ! <MODULE> 2
92   ! VTSAT       VTSN_1.2,BTN_1.2     :N  20/1.2     10,15,16,14
93   ! IDSAT       IDSN_20/1.2          :N  20/1.2     10,15,16,14
95   ! LEAK        LEAKN_20/1.2         :N  20/1.2     10,15,16,14
96   ! VTSAT       VTSN_1.6,BTN_1.6     :N  20/1.6      9,15,16,14
97   ! IDSAT       IDSN_20/1.6          :N  20/1.6      9,15,16,14
99   ! LEAK        LEAKN_20/1.6         :N  20/1.6      9,15,16,14
100! VTSAT         VTSN_20,BTN_20       :N  20/20      11,15,16,14
101! IDSAT         IDSN_20/20           :N  20/20      11,15,16,14
103! LEAK          LEAKN_20/20          :N  20/20      11,15,16,14
104! VTSAT         VTSP_1.2,BTP_1.2     :P  20/1.2     21,15,16,17
105! IDSAT         IDSP_20/1.2          :P  20/1.2     21,15,16,17
107! LEAK          LEAKP_20/1.2         :P  20/1.2     21,15,16,17
108! VTSAT         VTSP_1.6,BTP_1.6     :P  20/1.6     22,15,16,17
109! IDSAT         IDSP_20/1.6          :P  20/1.6     22,15,16,17
111! LEAK          LEAKP_20/1.6         :P  20/1.6     22,15,16,17
112! VTSAT         VTSP_20,BTP_20       :P  20/20      20,15,16,17
113! IDSAT         IDSP_20/20           :P  20/20      20,15,16,17
115! LEAK          LEAKP_20/20          :P  20/20      20,15,16,17
116 ! <MODULE> 3
117 ! RESZP        P+CONTACTS           :P  1.2X1.2    11,16
118 ! RESZP        N+CONTACTS           :N  1.2X1.2    10,16
119 ! RESZP        POLY_CTS             :N  1.1X1.2     9,16
120 ! RESZP        100x100_PR           :N  100x100    15,16
121 ! RESZP        2x100_PR             :N  1.2X100    14,16
122 ! RESZP        VIA_R                :N  1.6X1.6    17,16
123 ! CV0          GATE_CAP             :N  70x70      22,21,20
149 ! END
```


Fab E C12 Process
Parameter: VTN
October 1991
1.00E+00
9.50E-01
9.00E-01
8.50E-01
8.00E-01
7.50E-01
7.00E-01
6.50E-01
6.00E-01
VTN (volts)
Target=0.80
UCL=0.95
LCL=0.65
2-Oct-91
2-Oct-91
2-Oct-91
4-Oct-91
8-Oct-91
9-Oct-91
9-Oct-91
9-Oct-91
9-Oct-91
11-Oct-91
13-Oct-91
13-Oct-91
13-Oct-91
13-Oct-91
13-Oct-91
13-Oct-91
13-Oct-91
15-Oct-91
15-Oct-91
15-Oct-91
15-Oct-91
15-Oct-91
19-Oct-91
22-Oct-91
22-Oct-91
22-Oct-91
22-Oct-91
22-Oct-91
26-Oct-91
27-Oct-91
28-Oct-91
28-Oct-91
28-Oct-91
28-Oct-91
28-Oct-91
29-Oct-91
PCM Test Date
Cp=2.11 Cpk=1.72 Ns=838 Bave=0.827 Bmin=0.662 Bmax=0.936 Bsig=0.0237 SigDD=0.0178 SigWW=0.00237 SigLL=0.0156

FAB_E Lot 6613 (Ziggy)

DATA BASE STATISTICS REPORT

FAB E ELECTRICAL PARAMETER STATISTICS
Test Plan D
1 Jan 1000 to 1 Jan 2500

PARAMETER	AVERAGE	SIGMA	Cp	Cpk	TARGET	TOLERANCE
C10_M1-M1	-2.5E-11	+1.2E-10	+7.2E+03	+1.4E+01	+1.0E-10	
C10_M2-M2	-9.0E-10	+3.4E-09	+4.8E-01	+4.0E-01	+1.0E-10	
C12_M1-M1	-8.7E-12	+1.0E-10	+8.1E+03	+1.6E+01	+1.0E-10	
C12_M2-M2	+4.5E-11	+1.8E-10	+9.3E+03	+9.4E+00	+1.0E-10	
C10_M1-CON	+1.0E+02	+1.7E+00	+2.4E+01	+1.0E+01	+1.5E+02	
C10_M2-CON	+1.8E+01	+3.0E-01	+1.6E+02	+9.2E+00	+5.0E+01	
C12_M1-CON	+2.1E+02	+1.5E+02	+3.4E-01	+2.4E-01	+1.8E+02	
C12_M2-CON	+2.4E+01	+4.7E-01	+2.1E+02	+2.7E+00	+1.0E+02	
VTSN_1.2D	+8.3E-01	+9.9E-03	+5.1E+00	+3.9E+00	+8.0E-01	
BTN_1.2	+1.2E-03	+2.5E-05	+6.0E+00	+1.3E+00	+1.3E-03	
IDSN_1.2	+4.4E-03	+5.5E-05	+1.2E+01	+9.4E+00	+4.0E-03	
LEAKN_1.2	+1.7E-04	+6.4E-04	+5.2E-02	+1.4E-02	+2.0E-06	
VTSN_1.6	+8.4E-01	+9.3E-03	+1.3E+01	+1.2E+01	+8.0E-01	
BTN_1.6	+8.1E-04	+1.3E-05	+2.0E+01	+1.0E+01	+9.0E-04	
IDSN_1.6	+3.7E-03	+4.2E-05	+1.2E+01	+5.8E+00	+4.0E-03	
LEAKN_1.6	+3.5E-10	+1.3E-10	+1.3E+05	+1.4E+01	+1.0E-06	
VTSN_20	+8.9E-01	+9.9E-03	+1.8E+01	+1.7E+01	+9.5E-01	
BTN_20	+5.6E-05	+5.1E-07	+1.5E+02	+1.0E+01	+7.6E-05	
IDSN_20	+4.4E-04	+5.4E-06	+3.1E+00	+2.3E+00	+4.5E-04	
LEAKN_20	+1.8E-10	+6.7E-11	+2.5E+03	+2.6E+01	+5.0E-09	
VTSP_1.2	-7.4E-01	+9.3E-03	+5.4E+00	+3.3E+00	-8.0E-01	
BTP_1.2	+5.7E-04	+1.5E-05	+2.7E+00	+3.8E-01	+6.0E-04	
IDSP_1.2	-2.8E-03	+5.7E-05	+7.3E+00	+4.3E+00	-3.0E-03	
LEAKP_1.2	-2.5E-10	+3.4E-11	+2.5E+03	+5.1E+01	-5.0E-09	
VTSP_1.6	-8.1E-01	+4.8E-03	+2.9E+01	+2.7E+01	-8.5E-01	
BTP_1.6	+3.5E-04	+7.1E-06	+3.5E+01	+1.2E+01	+4.5E-04	
IDSP_1.6	-1.9E-03	+2.9E-05	+2.9E+00	+2.0E+00	-2.0E-03	
LEAKP_1.6	-1.3E-10	+2.4E-11	+3.8E+01	+5.2E+00	-1.0E-10	
VTSP_20	-8.7E-01	+6.5E-03	+4.6E+01	+3.4E+01	-9.8E-01	
BTP_20	+1.7E-05	+1.0E-07	+1.8E+02	+2.3E+01	+2.3E-05	
IDSP_20	-1.2E-04	+5.4E-07	+1.9E+01	+1.5E+01	-1.3E-04	
LEAKP_20	-1.8E-10	+2.2E-11	+4.6E+01	+1.3E+01	-1.5E-10	
P+CONTACTS	+7.3E+03	+4.5E+02	+3.0E+00	+2.0E+00	+7.0E+03	
N+CONTACTS	+9.9E+02	+3.7E+00	+6.5E+02	+2.6E+01	+1.5E+03	
POLY_CTS	+1.7E+03	+1.1E+02	+1.7E+01	+2.2E+00	+1.8E+03	
100x100_PR	+2.6E+01	+3.3E-01	+4.0E+02	+1.6E+01	+3.5E+01	
2x100_PR	+8.6E+02	+1.2E+01	+3.7E+00	+3.3E+00	+8.2E+02	
VIA_R	+4.3E+01	+8.8E-01	+2.8E+02	+5.1E+00	+8.0E+01	
GATE_CAP	+2.7E-12	+1.4E-14	+3.9E+01	+3.3E+01	+2.3E-12	

```
*** VARIATIONS REPORT ***
    Die-to-Die, Wafer-to-wafer, Lot-to-Lot and Total Sigmas by Parameter
C10_M1-M1   N:  15 D-D: +1.28E-10 W-W: +5.38E-11 L-L: +0.00E+00 Tot: +1.16E-10
C10_M2-M2   N:  15 D-D: +3.57E-09 W-W: +2.05E-10 L-L: +0.00E+00 Tot: +3.56E-09
C12_M1-M1   N:  15 D-D: +1.08E-10 W-W: +1.96E-11 L-L: +0.00E+00 Tot: +1.06E-10
C12_M2-M2   N:  15 D-D: +1.91E-10 W-W: +5.70E-11 L-L: +0.00E+00 Tot: +1.83E-10
C10_M1-CON  N:  14 D-D: +1.70E+00 W-W: +7.07E-01 L-L: +0.00E+00 Tot: +1.84E+00
C10_M2-CON  N:  14 D-D: +3.32E-01 W-W: +1.23E-01 L-L: +0.00E+00 Tot: +3.09E-01
C12_M1-CON  N:  15 D-D: +1.54E+02 W-W: +1.29E+01 L-L: +0.00E+00 Tot: +1.54E+02
C12_M2-CON  N:  14 D-D: +4.04E-01 W-W: +3.17E-01 L-L: +0.00E+00 Tot: +5.14E-01
VTSN_1.2D   N:  14 D-D: +1.11E-02 W-W: +4.99E-03 L-L: +0.00E+00 Tot: +9.90E-03
BTN_1.2     N:  14 D-D: +2.55E-05 W-W: +4.46E-06 L-L: +0.00E+00 Tot: +2.58E-05
IDSN_1.2    N:  14 D-D: +5.94E-05 W-W: +2.01E-05 L-L: +0.00E+00 Tot: +5.59E-05
LEAKN_1.2   N:  15 D-D: +6.67E-04 W-W: +8.22E-08 L-L: +0.00E+00 Tot: +6.67E-04
VTSN_1.6    N:  14 D-D: +1.02E-02 W-W: +4.02E-03 L-L: +0.00E+00 Tot: +9.37E-03
BTN_1.6     N:  14 D-D: +1.40E-05 W-W: +2.54E-06 L-L: +0.00E+00 Tot: +1.38E-05
IDSN_1.6    N:  15 D-D: +4.51E-05 W-W: +1.42E-05 L-L: +0.00E+00 Tot: +4.29E-05
LEAKN_1.6   N:  15 D-D: +1.39E-10 W-W: +4.93E-11 L-L: +0.00E+00 Tot: +1.30E-10
VTSN_20     N:  15 D-D: +1.11E-02 W-W: +4.83E-03 L-L: +0.00E+00 Tot: +9.94E-03
BTN_20      N:  15 D-D: +5.42E-07 W-W: +1.60E-07 L-L: +0.00E+00 Tot: +5.18E-07
IDSN_20     N:  15 D-D: +5.90E-06 W-W: +2.40E-06 L-L: +0.00E+00 Tot: +5.39E-06
LEAKN_20    N:  15 D-D: +7.34E-11 W-W: +2.80E-11 L-L: +0.00E+00 Tot: +6.79E-11
VTSP_1.2    N:  15 D-D: +1.03E-02 W-W: +4.42E-03 L-L: +0.00E+00 Tot: +9.29E-03
BTP_1.2     N:  15 D-D: +1.52E-05 W-W: +1.99E-06 L-L: +0.00E+00 Tot: +1.53E-05
IDSP_1.2    N:  15 D-D: +5.99E-05 W-W: +9.03E-06 L-L: +0.00E+00 Tot: +5.92E-05
LEAKP_1.2   N:  15 D-D: +3.72E-11 W-W: +1.43E-11 L-L: +0.00E+00 Tot: +3.43E-11
VTSP_1.6    N:  15 D-D: +5.30E-03 W-W: +2.01E-03 L-L: +0.00E+00 Tot: +4.90E-03
BTP_1.6     N:  15 D-D: +7.72E-06 W-W: +2.63E-06 L-L: +0.00E+00 Tot: +7.26E-06
IDSP_1.6    N:  15 D-D: +3.02E-05 W-W: +6.18E-06 L-L: +0.00E+00 Tot: +2.95E-05
LEAKP_1.6   N:  15 D-D: +2.11E-11 W-W: +1.58E-11 L-L: +0.00E+00 Tot: +2.63E-11
VTSP_20     N:  15 D-D: +7.07E-03 W-W: +2.39E-03 L-L: +0.00E+00 Tot: +6.66E-03
BTP_20      N:  15 D-D: +1.08E-07 W-W: +3.55E-08 L-L: +0.00E+00 Tot: +1.02E-07
IDSP_20     N:  15 D-D: +5.50E-07 W-W: +8.24E-08 L-L: +0.00E+00 Tot: +5.56E-07
LEAKP_20    N:  15 D-D: +2.37E-11 W-W: +9.28E-12 L-L: +0.00E+00 Tot: +2.18E-11
P+CONTACTS  N:  15 D-D: +4.49E+02 W-W: +1.46E+02 L-L: +0.00E+00 Tot: +4.72E+02
N+CONTACTS  N:  15 D-D: +3.24E+00 W-W: +2.38E+00 L-L: +0.00E+00 Tot: +4.03E+00
POLY_CTS    N:  15 D-D: +1.16E+02 W-W: +2.38E+01 L-L: +0.00E+00 Tot: +1.13E+02
100x100_PR  N:  15 D-D: +2.73E-01 W-W: +2.43E-01 L-L: +0.00E+00 Tot: +3.65E-01
2x100_PR    N:  15 D-D: +1.25E+01 W-W: +3.80E+00 L-L: +0.00E+00 Tot: +1.19E+01
VIA_R       N:  15 D-D: +7.22E-01 W-W: +6.67E-01 L-L: +0.00E+00 Tot: +9.83E-01
GATE_CAP    N:  15 D-D: +1.53E-14 W-W: +6.77E-15 L-L: +0.00E+00 Tot: +1.37E-14
```

LOT SUMMARY BY PARAMETER WHERE MIN AND MAX VALUE OF PARAMETER OCCURRED

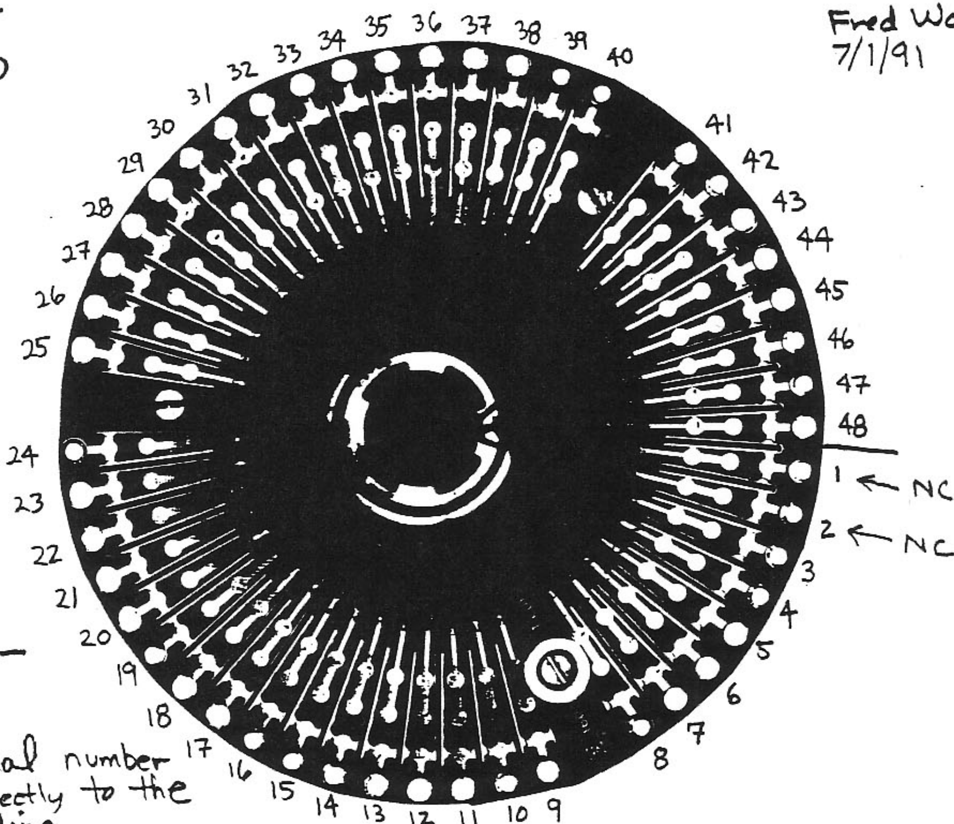
PARAMETER		MINIMUM		MAXIMUM
C10_M1-M1	6613-Eng1	-3.6200E-10	6613-Eng1	1.5908E-10
C10_M2-M2	6613-Eng1	-1.3770E-08	6613-Eng1	1.7604E-10
C12_M1-M1	6613-Eng1	-1.5896E-10	6613-Eng1	2.3740E-10
C12_M2-M2	6613-Eng1	-1.3634E-10	6613-Eng1	6.4380E-10
C10_M1-CON	6613-Eng1	9.9540E+01	6613-Eng1	1.0636E+02
C10_M2-CON	6613-Eng1	1.7989E+01	6613-Eng1	1.8800E+01
C12_M1-CON	6613-Eng1	1.6277E+02	6613-Eng1	7.6449E+02
C12_M2-CON	6613-Eng1	2.3186E+01	6613-Eng1	2.4410E+01
VTSN_1.2D	6613-Eng1	8.1349E-01	6613-Eng1	8.4717E-01
BTN_1.2	6613-Eng1	1.1442E-03	6613-Eng1	1.2337E-03
IDSN_1.2	6613-Eng1	4.3776E-03	6613-Eng1	4.5462E-03
LEAKN_1.2	6613-Eng1	2.3916E-10	6613-Eng1	2.5822E-03
VTSN_1.6	6613-Eng1	8.2160E-01	6613-Eng1	8.5642E-01
BTN_1.6	6613-Eng1	7.8048E-04	6613-Eng1	8.2786E-04
IDSN_1.6	6613-Eng1	3.6768E-03	6613-Eng1	3.7956E-03
LEAKN_1.6	6613-Eng1	2.1552E-10	6613-Eng1	6.5176E-10
VTSN_20	6613-Eng1	8.6955E-01	6613-Eng1	9.0213E-01
BTN_20	6613-Eng1	5.5113E-05	6613-Eng1	5.6863E-05
IDSN_20	6613-Eng1	4.3088E-04	6613-Eng1	4.4864E-04
LEAKN_20	6613-Eng1	8.7200E-11	6613-Eng1	3.4840E-10
VTSP_1.2	6613-Eng1	-7.6540E-01	6613-Eng1	-7.2789E-01
BTP_1.2	6613-Eng1	5.4608E-04	6613-Eng1	6.0522E-04
IDSP_1.2	6613-Eng1	-2.8722E-03	6613-Eng1	-2.6410E-03
LEAKP_1.2	6613-Eng1	-3.0676E-10	6613-Eng1	-2.0374E-10
VTSP_1.6	6613-Eng1	-8.2383E-01	6613-Eng1	-8.0369E-01
BTP_1.6	6613-Eng1	3.3897E-04	6613-Eng1	3.6660E-04
IDSP_1.6	6613-Eng1	-1.9728E-03	6613-Eng1	-1.8598E-03
LEAKP_1.6	6613-Eng1	-1.7716E-10	6613-Eng1	-1.0174E-10
VTSP_20	6613-Eng1	-8.8502E-01	6613-Eng1	-8.6220E-01
BTP_20	6613-Eng1	1.6909E-05	6613-Eng1	1.7288E-05
IDSP_20	6613-Eng1	-1.2426E-04	6613-Eng1	-1.2244E-04
LEAKP_20	6613-Eng1	-2.1814E-10	6613-Eng1	-1.3652E-10
P+CONTACTS	6613-Eng1	6.5366E+03	6613-Eng1	8.2048E+03
N+CONTACTS	6613-Eng1	9.7781E+02	6613-Eng1	9.9200E+02
POLY_CTS	6613-Eng1	1.5948E+03	6613-Eng1	1.9616E+03
100x100_PR	6613-Eng1	2.5574E+01	6613-Eng1	2.6401E+01
2x100_PR	6613-Eng1	8.3357E+02	6613-Eng1	8.8141E+02
VIA_R	6613-Eng1	4.1994E+01	6613-Eng1	4.5197E+01
GATE_CAP	6613-Eng1	2.6410E-12	6613-Eng1	2.6770E-12

PCM Wafer Tester HP 4062C Channel Wiring

Fred Wahl
7/1/91

HEWLETT PACKARD
Personality Board
16072A

(as seen from above & as normally installed in the EG 2001 wafer prober)

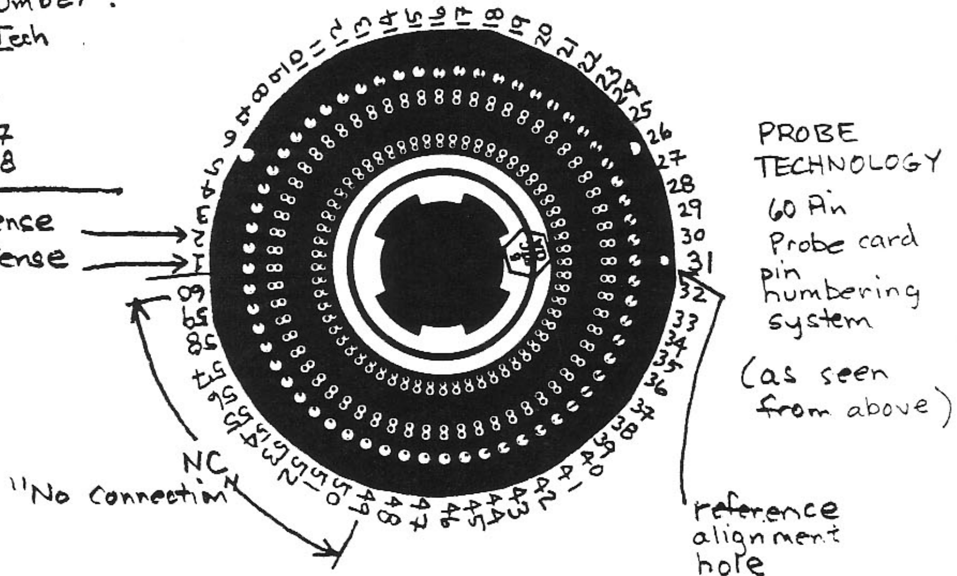


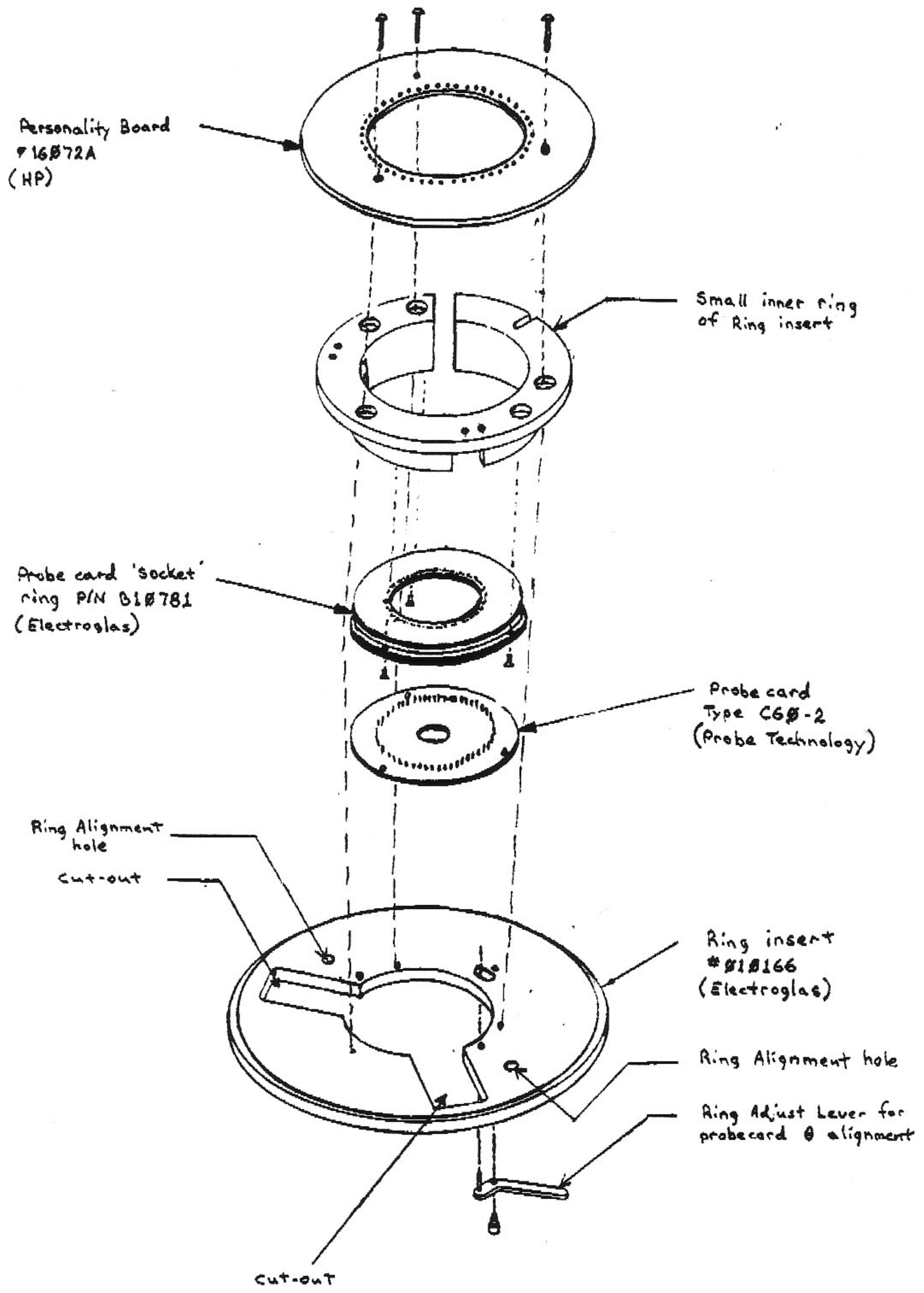
WIRING:

HP Terminal number wired directly to the corresponding PROBE TECHNOLOGY Terminal number:

HP	PTech
3 →	3
4 →	4
⋮	⋮
47 →	47
48 →	48

Edge Sense →
Edge Sense →





Personality Board
16Ø72A
(HP)
Small inner ring
of Ring insert
Probe card 'socket'
ring P/N B1Ø781
(Electroglas)
Probe card
Type C6Ø-2
(Probe Technology)
Ring Alignment
hole
Cut-out
Ring insert
#Ø1Ø166
(Electroglas)
Ring Alignment hole
Ring Adjust Lever for
probecard θ alignment
Cut-out