BSIM, a compact model for MOS transistors

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Abstract

The BSIM model (Berkeley Short channel Igfet Model) is presented and discussed. A BSIM parameter extraction method using TMA's TOPEX is outlined.

Introduction

The need for accurate transistor models has long been appreciated by the circuit design community. Transistor models coded into circuit simulation programs such as SPICE or SLIC have often limited the designer's ability to correctly predict circuit performance. Because of this, there has been a steady evolutionary pressure to improve these models.

Integrated circuit designers have seen the evolution of the Berkeley SPICE MOS models through levels 1, 2 and 3 [2]. Recently the U.C. Berkeley Electronics Research Lab has made available the BSIM model for use in SPICE [4]. This report describes the BSIM model and how BSIM transistor parameters may be extracted using TMA's general parameter extraction program, TOPEX.

BSIM general background

The BSIM model predicts drain terminal current and transistor capacitances as a function of the control voltages on the gate, drain, bulk and source terminals. Other inputs to the model include the transistor's channel width and length and its temperature. The computed capacitances have been modeled so that charge is conserved—thus helping convergence and accuracy of the circuit simulator.

The BSIM model falls into the category which deGraaff and Klaassen call compact semi-empirical models [1]. It is an analytical model comprised of a sequence of equations which originally were derived from device physical considerations but which have subsequently been modified empirically to achieve better fit to measured data. As in other models of this type [3, 2, 1], embedded in the equations are constants (parameters) which give the model a specific behavior. The term "compact" applies because the model designer's goal was to use as few equations as possible so that circuit simulator speed would be enhanced.

BSIM incorporates into its design the concept of a two-stage model, which has proven successful in other accurate proprietary models [7]. The first stage interfaces to the circuit simulator and "preprocesses" the various temperature and device geometry requests into specific transistor physical model parameters. The second stage takes these specific transistor physical parameters and uses them to compute currents and capacitances.

For each transistor type (e.g. N channel enhancement) from a particular semiconductor manufacturing process, a single geometry-independent parameter set results which the circuit simulator can use to predict the performance of any geometry transistor. This BSIM parameter set is in a sense a function only of the semiconductor processing. It is therefore understandable why the BSIM parameter file is known as a "Process" file.

The focus of the following discussion of the BSIM equations will be to provide an understanding of how its parameters may be extracted using TMA's TOPEX. The developers of BSIM intended that its parameters would be extracted using an automated test and data analysis system. This automation would provide a means of acquiring sufficient volumes of parameter data needed for statistical modeling of circuit performance variations. Such a system was created at

U.C. Berkeley [6, 5]. The system was based upon custom software which performs cycles of testing alternating with parameter extraction calculations.

TMA has developed a methodology using separate testing and subsequent parameter optimization using TOPEX which now makes BSIM modeling practical.

The BSIM model equations from a parameter extraction perspective

Appendix A lists the BSIM model equations for the DC portion of the model. The equations as shown are to be evaluated from left to right and from top to bottom. Also provided is a table which lists and describes the variables used in the equations. We will save a discussion of the capacitance portions of the model for another occassion. For a complete discussion and derivation of the model equations the interested reader is referred to a paper by Sheu, Scharfetter, Ko and Jeng [4].

The input parameters which BSIM recognizes are shown as variables whose names are entirely in uppercase characters. All other variables in the model equations are either physical constants, internal parameters or control voltages.

In equations (1) and (2) the extrinsic source and drain series resistors are computed. The number of squares of source-drain diffusion are generally determined from the layout of the transistor. It is important to extract the source-drain sheet resistance at an early stage so that the value of U_0 models the intrinsic channel only.

Equation (5) is where most of the transistor geometry dependence enters the BSIM model. For each of the internal parameters represented using this equation, the formulation can be visualized as a plane in three dimensions, modeling the transistor specific parameter data as a function of the reciprocal of the effective gate width and length for each transistor. $PARM_i$ represents the plane's parameter "value" over the origin and $WPARM_i$ and $LPARM_i$ represent the plane's width and length dependent "slopes." The value $PARM_i$ corresponds to that for an infinitely large transistor. Nineteen of the internal BSIM parameters are treated in this fashion (see the parameters annotated with a † in Appendix A for a complete list). For example, V_{FB} obeys the equation:

$$V_{FB}(W,L) = VFB + \frac{WVFB}{W_{eff}} + \frac{LVFB}{L_{eff}}$$

Note that if the data from one specific geometry transistor is used to fit a version of the model where all the $WPARM_i$ and $LPARM_i$ are forced to zero, then the resulting extracted parameters will be for that specific geometry device only. Highly accurate models result using BSIM to fit the data from specific geometry transistors in this way. If this is how one wished to use the model, then each geometry transistor would require a separate set of BSIM parameters, however.

In practice we want a single BSIM model to predict the behavior of all

transistor geometries. For a given transistor type we therefore want valid values of all the $PARM_i$, $WPARM_i$ and $LPARM_i$. As the example that follows demonstrates, this is done using TOPEX by first extracting parameters for a set of specific geometry transistors one at a time. Parameters from this fitting are then used as input data in a fit which uses the plane geometry model discussed previously.

The bias-dependent mobility, equation (6), is better understood by looking at some of its limits. If we first ignore back bias effects by setting V_{BS} to zero, we see that the "low field" limit is:

$$\lim_{\frac{V_{DS}}{V_{DD}} \to 0} \mu = \mu_Z$$

and the limit at the high drain reference voltage becomes:

$$\lim_{\frac{V_{DS}}{V_{DD}} \to 1} \mu = \mu_S$$

In other words, as the drain voltage increases the mobility makes a transition from the low field value, μ_Z, to the high field value μ_S. It can also be shown that at the high field limit the slope of the mobility curve is given by:

$$\lim_{\frac{V_{DS}}{V_{DD}} \to 1} \frac{\partial \mu}{\partial V_{DS}} = \mu_{SD}$$

Thus with three parameters a simple curved function of V_{DS} is produced which describes mobility variation. If we now restore the back bias dependent terms in the mobility equation, we see that the parameters μ_{ZB} and μ_{SB} simply serve to modify the low field and high field mobilities respectively in a manner proportional to back bias. These facts suggest bias ranges within which the related parameters should be extracted. Furthermore they suggest a particular sequence of extraction of these same parameters.

Other geometry dependencies in the BSIM model are tightly linked with bias dependencies. One strongly bias and geometry influenced parameter is β as computed from equations (6) and (7). Note that the gain factor, β, in the limit of small drain and bulk biases, approaches a term familiar to those who model MOS transistors:

$$\lim_{V_{BS},V_{DS}\to 0} \beta(W,L) = \mu_0 C_{ox} \left(\frac{W_{eff}}{L_{eff}} \right)$$

This fact will prove useful when we extract the parameters MUZ(μ_0 or μ_Z), DL(delta L) and DW(delta W) using data from the "linear" region of transistor behavior.

The equation describing the threshold voltage, equation (12), deserves some comment from the point of view of parameter extraction. V_{th} is the gate voltage at which the transistor enters "strong inversion' channel conduction. Most process technologists are familiar with V_{th}. In fact it is often used as a process monitoring and control variable. Historically the "extrapolated" threshold voltage has been used for this purpose and is computed by fitting the "strong inversion" portion of the I_D versus V_{GS} characteristic with either a line or a parabola and then extrapolating the curve to where it intersects the voltage axis at zero amperes. For small V_{DS} this "extrapolated" V_{th} closely approximates the BSIM V_{th}.

Unfortunately BSIM hides V_{th} as an internal parameter. For purposes of comparing extracted model parameters with normal process control data we may estimate V_{th} for the zero volt back bias and low voltage drain case by:

$$V_{th} \approx V_{FB} + \phi_S$$

For small V_{DS} we note that the parameters K_1 and K_2 can be viewed as causing a shift in V_{th} as a function of back bias. This suggests we extract these parameters using "linear" region data. The parameter η, the drain induced barrier lowering factor, influences several regions of transistor behavior, but is a minor player in the "linear" region because of the assumed small value of V_{DS}.

Consequences of a numerical approximation to assure accurate body effect predictions over a wide range of drain and substrate voltages are seen in equations (13) through (17). The reader is referred to Sheu, et al [4] for a detailed description. Experience using the model shows the success of the approximation which results in better fitting in the triode and saturation regions as compared to the previous MOS SPICE models.

We thus finally enter the actual drain current computations of the BSIM model. Here we find that depending upon the transistor bias, different formulations apply. The bias on the gate of the transistor determines if it is operating in "strong" inversion or not. If $V_{GS} > V_{th}$ then the transistor operates in strong inversion and either equation (18), the triode region behavior, or (19), the saturation region behavior, will apply. The voltage on the drain of the transistor selects between these two cases. If $V_{DS} \geq V_{DSAT}$ then equation (19) prevails.

The "triode" region of behavior has a special case which we have mentioned several times before in the previous discussion. For small V_{DS} the triode drain current expression simplifies to an approximation which is a linear function of the the "gate overdrive voltage," $V_{GS} - V_{th}$. In practice a constant $V_{DS} = 0.1$ or 0.2 volt is used to force the transistor to operate in the "linear" region. Data collected from this region of behavior will be used in the extraction of many of our BSIM parameters. The upper reaches of the triode characteristic, where V_{DS} is not small but is still less than V_{DSAT} is well modeled by BSIM. Data from this portion of the triode region is often grouped with the data from the "saturation" region to produce the most satisfying overall fits.

In equation (19) for the "saturation" region of behavior we see the familiar dependence on the

square of the "gate overdrive voltage." Note that the body effect and the velocity saturation effects enter through the $2aK$ term. Output conductance is controlled by the drain induced barrier lowering and velocity saturation parameters.

When the gate voltage falls below the threshold voltage, the strong inversion component of the drain current shuts off and current flow is due to "weak" inversion mechanisms. The transistor is said to operate in the "Subthreshold" region. Equations (21) through (24) are used to describe the resulting drain current in the BSIM model. In this region of behavior both V_{DS} and V_{BS} may assume the same large voltages as in the saturation region. Since these large voltages are possible, the drain induced barrier lowering and subthreshold slope parameters become important in subthreshold. Drain induced barrier lowering is important because it significantly shifts V_{th} which causes a lateral translation of the characteristic. Note that the subthreshold slope parameter, n, enters through equation (22). When the low values of drain current from this region are plotted on $log(I_D)$ vs V_{GS} graphs the slope which this parameter controls may be observed. Large values of n cause shallow slopes and small values cause steep slopes.

Attempts to control the continuity problem which results when crossing into the subthreshold region can be seen in the $\exp^{1.8}$ term in equation (22) and the current limiting summarized in equation (23). Note that when the exponential current, I_{exp}, becomes much larger than the limiting current, then the limiting current, I_{limit} becomes the effective current. Conversely only when $I_{exp} \ll I_{limit}$ does the curve normally used to describe subthreshold behavior appear. The BSIM modeling of subthreshold is not yet perfect but it does a reasonably good job when its limitations are understood, and it performs better than previous versions of MOS SPICE.

Extracting BSIM parameters using TMA's TOPEX

The following sections of this paper illustrate the major stages of an automated BSIM parameter extraction method developed for use with TMA's TOPEX program. Transistor test data was collected using a commercial test system which was instructed to format the test data for use with TOPEX. TMA has created application note guidelines showing its customers how to prepare test data for TOPEX [9, 10]. Once the datafile has been prepared, TOPEX is used in conjunction with a control command file or "strategy" file to extract parameters. An understanding of the BSIM model as discussed above was used to develop an example extraction "strategy" file. This example is provided to those who license TOPEX and is further documented in the TOPEX manual [8].

Where applicable, each step of the extraction process is illustrated with either a "diagnostic" or "verification" plot. The "diagnostic" plots are used to observe the fitting process as it proceeds. "Verfication" plots are used to check the model fit once all parameters have been determined. It is believed that this graphical approach is the best way to show the excellent fitting that is possible using TOPEX and BSIM.

All these plots were created by TOPEX and show the test data as plus symbols and the current status of the fitted BSIM model using curves. Control voltage biases are shown as comments on each graph. Also the titles of diagnostic plots usually indicate which region of transistor behavior is being targeted and also contain a strategy sequence number used to identify the specific extraction used.

Extracting the "Core" parameters

A small handful of the BSIM model parameters are so fundamental and physically based that they should be extracted at the earliest possible moment. The success of the following extractions will pivot on the accuracy of these parameters. Figure 1 shows the results of extracting the zero bias mobility(MUZ), delta L(DL), delta W(DW) and the source drain sheet resitivity(RSH). These parameters are treated as being constant for all device sizes at a given location on the silicon wafer. The gate oxide thickness was assumed known from process information, and the number of squares of source and drain were

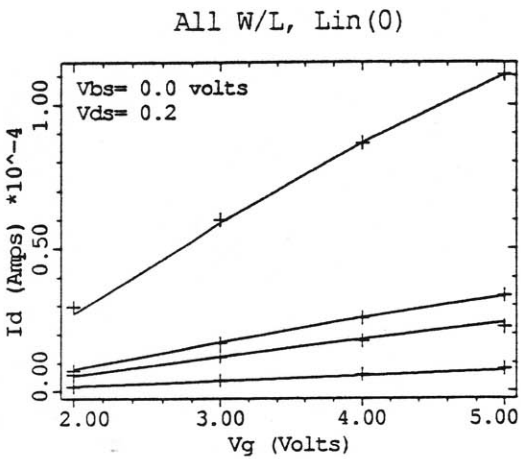

Figure 1: Extracting the "core" parameters MUZ, DL, DW and RSH.Values for TOX, NRS and NRD were known already.

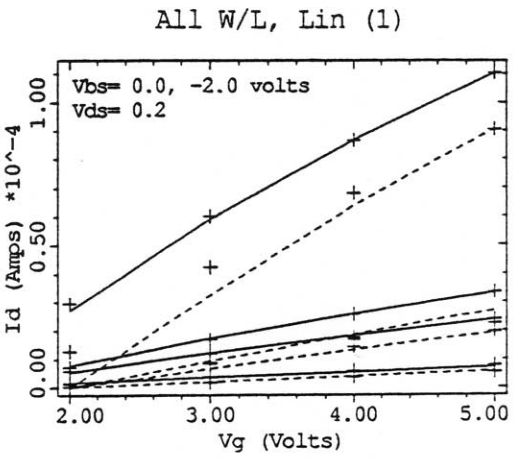

Figure 2: A preliminary fit of the Linear data is done to get a better estimateof K1, PHI and VFB. The dashed lines are for $V_{BS} = -2.0$ volts.

calculated from the device layout. Each curve corresponds to the model fit to four data points from a specific transistor. From top to bottom these curves represent the fit to data from the "linear" region for the 10/3, 3/3, 20/20, and 3/10 micron devices. Again, for a complete description of the extraction method, the reader is referred to the TOPEX manual [8].

Next we again extract using data from all transistor geometries to get a better initial guess for certain parameters used in the subsequent device specific extractions. A better estimate of the average $K1$, VFB and PHI are needed. Figure 2 shows the diagnostic fit plot after the optimization was performed. The dashed lines show the model fit to added test data associated with $V_{BS} = -2$ volts.

Extracting the Device Specific Parameters

At this stage of the extraction we determine and save the physical or internal parameters for each specific geometry transistor that we have tested. These saved parameters will be used later when they are fit with the BSIM geometrical scaling model as discussed in the next section. The TOPEX strategy file performs looping so that all devices are analyzed. We present here examples only for one of the devices.

The first extraction that we perform gets device specific parameters VFB, K1, U0 and X2U0. Normally we would also extract K2 at this time, but more back biases are required to determine K2 accurately. Figure 3 shows the resulting diagnostic fit verification plot for the 20/20 device.

The next device-specific extraction focuses on the saturation region using zero volt back bias data only. Here the parameters MUS, X3MS, U1, X3U1, ETA and X3E are determined. The resulting fit can be observed in Figure 4.

The next step in our parameter extraction strategy process is to again look at saturation region data, but this time we will add data for $V_{BS} = -2$ to what we used previously. Now parameters influenced by back bias effects which dominate in the saturation and upper triode regions are extracted. These parameters are X2MZ, X2MS, X2E and X2U1. Figure 5 shows the fit which results after extracting these parameters for the 20/20 device.

The last three extractions are repeated for the other transistors. Once this is complete we may then extract the BSIM parameters which will contain the transistor geometry scaling.

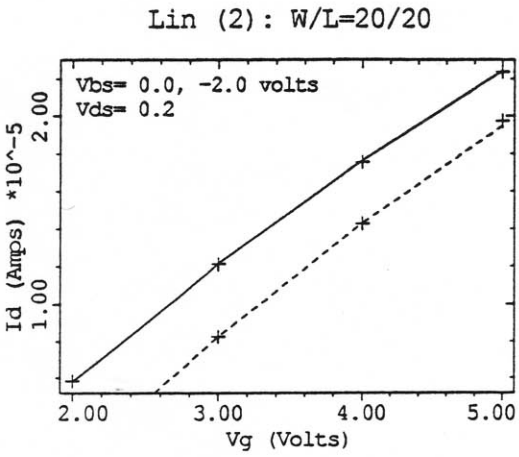

Figure 3: The first device specific fit. Here a W/L=20/20 transistor is examined and VFB, K1, U0 and X2U0 are determined for it.

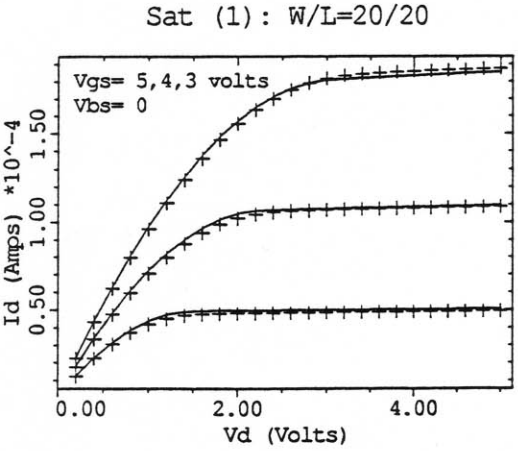

Figure 4: The second device specific fit. Here the W/L=20/20 transistor is presented as fit using parameters MUS, X3MS, U1, X3U1, ETA and X3E.

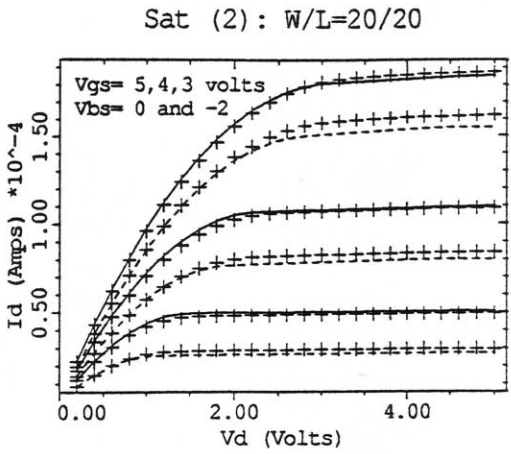

Figure 5: The third device specific fit. Here a W/L=20/20 transistor is examined and X2MZ, X2MS, X2E and X2U1 are determined for it.

Extracting the Process Block Parameters

In this step we determine the parameters which become the final geometry independent process file. In this step 19 of the BSIM physical or internal parameters will be replaced by three parameters each. As you recall from the earlier discussion VFB is one of these 19. It will be replaced in the final BSIM process block parameter file with the three parameters VFB, WVFB and LVFB. These three parameters are used by SPICE to predict the physical VFB parameter for any W/L gate dimension transistor.

No plot is shown for this extraction, but TOPEX is used to read back in the physical parameters determined in the previous section, to extract these new parameters, and to format an output file containing the BSIM parameters.

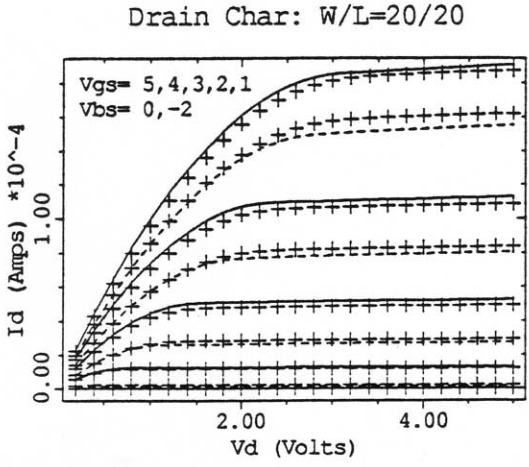

Figure 6: Verification Plot for the W/L=20/20 transistor showing the drain characteristics. The dashed lines are for $V_{BS} = -2$ volts.

Verifying Accuracy of Model Fit

To verify the overall fit that results, it is good practice to generate fit verification plots for each transistor geometry. Figures 6 through 9 show the fits for the four transistor geometries used. These plots were created by TOPEX as commanded from the same "strategy" file which has done all the previous work.

As you can see, the overall fit is excellent. We now have a BSIM model which is good for a wide range of transistor sizes.

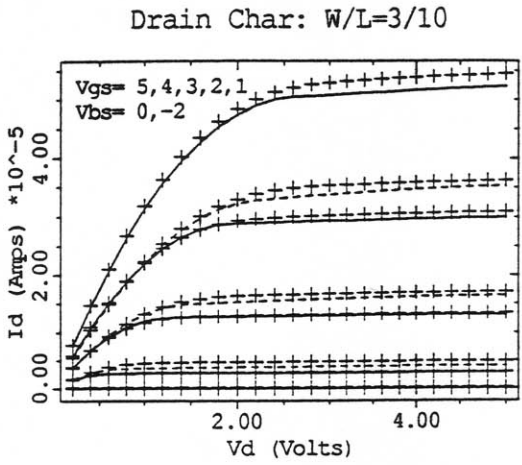

Figure 7: Verification Plot for the W/L=3/10 transistor showing the drain characteristics. The dashed lines are for $V_{BS} = -2$ volts.

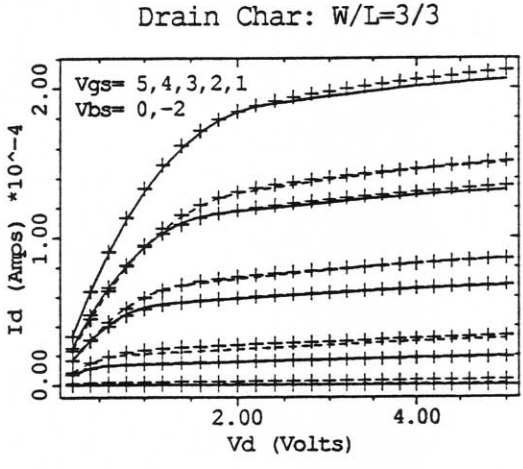

Figure 8: Verification Plot for the W/L=3/3 transistor showing the drain characteristics. The dashed lines are for $V_{BS} = -2$ volts.

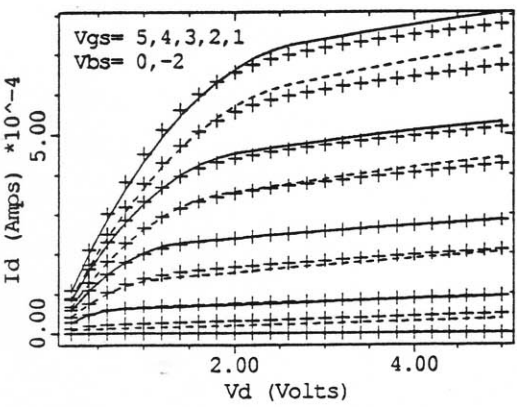

Figure 9: Verification Plot for the W/L=10/3 transistor showing the drain characteristics. The dashed lines are for $V_{BS} = -2$ volts.

Summary and Conclusions

Portions of the BSIM model dealing with DC transistor currents have been presented and discussed. A parameter extraction "strategy" using TMA's TOPEX and its implementation of BSIM 3b1 has been discussed and shown to accurately model MOS transistors.

A practical, commercially available method for extracting BSIM parameters is now available. Using one parameter extraction "strategy" file, we have shown that TOPEX can automatically generate the DC BSIM process parameters.

In addition, this example should serve as a flexible and powerful platform from which new parameter extraction "strategies" may be developed. The methodology outlined in this example is easily extended to generate large volumes of extracted parameters for purposes of statistical modeling.

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Appendix A: SPICE 3b1 BSIM DC Equations and Parameters

Geometry Related Parameters:

(1) $Rs = RSH \cdot NRS$; (2) $Rd = RSH \cdot NRD$

(3) $L_{eff} = L - DL$; (4) $W_{eff} = W - DW$

(5) $Parm_i(W,L) = PARM_i + \frac{WPARM_i}{W_{eff}} + \frac{LPARM_i}{L_{eff}}$ for $i = 1$ to 19 (see † in the following table)

Bias Dependent Internal or Physical Parameters:

Mobility: (6) $\mu = (\mu_Z + \mu_{ZB}V_{BS})\left(\frac{V_{DS}}{V_{DD}} - 1\right)^2 + (\mu_S + \mu_{SB}V_{BS})\left(2 - \frac{V_{DS}}{V_{DD}}\right)\frac{V_{DS}}{V_{DD}} + \mu_{SD}V_{DS}\left(\frac{V_{DS}}{V_{DD}} - 1\right)$

Gain factor: (7) $\beta \equiv \mu C_{ox}\frac{W_{eff}}{L_{eff}}$

Vertical field mobility degradation: (8) $U_0 = U_{0Z} + U_{0B}V_{BS}$

Velocity Saturation coefficient: (9) $U_1 = U_{1Z} + U_{1B}V_{BS} + U_{1D}(V_{DS} - V_{DD})$

Subthreshold-slope coefficient: (10) $n = n_o + n_B V_{BS} + n_D V_{DS}$

Drain-induced barrier lowering coefficient: (11) $\eta = \eta_0 + \eta_B V_{BS} + \eta_D(V_{DS} - V_{DD})$

Threshold Voltage: (12) $V_{th} = V_{FB} + \phi_S + K_1\sqrt{\phi_S - V_{BS}} - K_2(\phi_S - V_{BS}) - \eta V_{DS}$

Strong Inversion Drain Current Component:

(13) $g = 1 - \frac{1}{1.744 + 0.8364(\phi_s - V_{BS})}$; (14) $a = 1 + \frac{gK_1}{2\sqrt{\phi_s - V_{BS}}}$

(15) $v_c = \frac{U_1}{L_{eff}}\frac{(V_{GS} - V_{th})}{a}$; (16) $K = \frac{1 + v_c + \sqrt{1 + 2v_c}}{2}$

(17) $V_{DSAT} = \frac{V_{GS} - V_{th}}{a\sqrt{K}}$

(Triode Region (Linear when V_{DS} is small)) *If* ($V_{GS} > V_{th}$ and $0 < V_{DS} < V_{DSAT}$) *then*

(18) $I_{D,S} = \frac{\beta}{1 + U_0(V_{GS} - V_{th})} \cdot \frac{(V_{GS} - V_{th})V_{DS} - \frac{a}{2}V_{DS}^2}{\left(1 + \frac{U_1}{L_{eff}}V_{DS}\right)}$

(Saturation Region) *If* ($V_{GS} > V_{th}$ and $V_{DS} \geq V_{DSAT}$) *then*

(19) $I_{D,S} = \frac{\beta}{1 + U_0(V_{GS} - V_{th})} \cdot \frac{(V_{GS} - V_{th})^2}{2aK}$

(Cutoff Region) *If* ($V_{GS} \leq V_{th}$) *then*

(20) $I_{D,S} = 0$

Weak-Inversion Drain Current Component:

(Subthreshold Region) *Significant when* ($V_{GS} \leq V_{th}$)

(21) $I_{limit} = \frac{\beta}{2}\left(3\frac{kT}{q}\right)^2$

(22) $I_{exp} = \beta\left(\frac{kT}{q}\right)^2 \exp^{1.8}\exp^{(V_{GS} - V_{th})q/nkT}\left(1 - \exp^{-qV_{DS}/kT}\right)$

(23) $I_{D,W} = \frac{I_{exp}I_{limit}}{I_{exp} + I_{limit}}$

BSIM DC currents:

(24) $I_D = I_{D,S} + I_{D,W}$; (25) $I_S = -I_D$; (26) $I_G = I_B = 0$

SPICE 3b1 BSIM Model Parameters

SPICE Name	Symbol	Description
RSH	RSH	Drain and source diffusion sheet resistance (ohms/square)
NRS	NRS	Effective number of source diffusion squares
NRD	NRD	Effective number of drain diffusion squares
W	W	Transistor nominal or drawn channel width
L	L	Transistor nominal or drawn channel length
DL	DL	Channel shortening (delta L)
DW	DW	Channel narrowing (delta W)
TOX	t_{ox}	Gate oxide thickness (used to compute C_{ox})
TEMP	T	Temperature at which parameters were measured
VDD	V_{DD}	High-field reference drain-to-source voltage (usu. $V_{DD} \geq 5$ volts)
MUZ	μ_Z	Zero-bias mobility (μ_0)
X2MZ,WX2MZ,LX2MZ †	μ_{ZB}	Sensitivity of mobility to substrate bias at $V_{DS} = 0$
MUS,WMUS,LMUS	μ_S	Mobility at zero substrate bias and at $V_{DS} = V_{DD}$
X2MS,WX2MS,LX2MS	μ_{SB}	Sensitivity of mobility to substrate bias at $V_{DS} = V_{DD}$
X3MS,WX3MS,LZ3MS	μ_{SD}	Sensitivity of mobility to drain bias at $V_{DS} = V_{DD}$
U0,WU0,LU0	U_{0Z}	Zero-bias vertical-field mobility degradation coefficient
X2U0,WX2U0,LX2U0	U_{0B}	Sensitivity of vertical-field mobility degradation to substrate bias
U1,WU1,LU1	U_{1Z}	Zero-bias velocity saturation coefficient
X2U1,WX2U1,LX2U1	U_{1B}	Sensitivity of velocity saturation effect to substrate bias
X3U1,WX3U1,LX3U1	U_{1D}	Sensitivity of velocity saturation effect on drain bias at $V_{DS} = V_{DD}$
N0,WN0,LN0	n_0	Zero-bias subthreshold slope coefficient
NB,WNB,LNB	n_B	Sensitivity of subthreshold slope to substrate bias
ND,WND,LND	n_D	Sensitivity of subthreshold slope to drain bias
ETA,WETA,LETA	η_0	Zero-bias drain-induced barrier lowering (DIBL) coefficient
X2E,WX2E,LX2E	η_B	Sensitivity of DIBL effect to substrate bias
X3E,WX3E,LX3E	η_D	Sensitivity of DIBL effect to drain bias at $V_{DS} = V_{DD}$
VFB,WVFB,LVFB	V_{FB}	Flat-band voltage
PHI,WPHI,LPHI	ϕ_S	Surface inversion potential
K1,WK1,LK1	K_1	Body effect coefficient
K2,WK2,LK2	K_2	Drain/source depletion charge sharing coefficient

† The $PARM_i$, $WPARM_i$ and $LPARM_i$ begin here and continue to the bottom of the table