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Contour Maps Reveal Non-Uniformity In Semiconductor Processing

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Iso-sheet resistance and iso-thickness contour maps are presented which reveal distinctive patterns of non-uniformity in some of the standard processes used for fabricating devices in silicon wafers. Rapid data acquisition, analysis, and display techniques make it possible to employ wafer mapping not only for process development and research but for control purposes as well. An example is given of process control data obtained over a period of six months for 3 in. diameter ion-implanted silicon wafers.

THE FABRICATION OF DEVICES in silicon wafers involves a series of doping operations in conjunction with the growth and deposition of insulating films. In order to assure that a maximum number of devices will be functional and meet desired performance criteria, the variation of critical process parameters such as sheet resistance and film thickness must be carefully controlled.

An experimental assessment of the factors which influence the wafer homogeneity of a particular process generally requires the use of automated wafer-test and data processing equipment. Using values for the mean and standard deviation, one may make a statistically meaningful comparison between wafers processed under different conditions. With the addition of computer graphics techniques, the distribution of experimental data may be displayed in the form of frequency plots (histograms),[1,2] two-dimensional maps,[2-5] and three-dimensional perspective drawings.[1-3] In this paper, two-dimensional contour maps are employed for exhibiting the spatial variation of parameters such as sheet resistance and film thickness. This approach presents measurement data in a format which is easily comprehended not only by those performing the wafer characterization but by those responsible for maintaining or improving a particular semiconductor process.

Figure 1a illustrates a simple two-dimensional presentation of data which is the starting point for constructing contour maps. The numerical values (. . . −2, −1, 0, +1, +2, . . .) represent, rounded to the nearest integer, the per cent deviation from the mean sheet resistance for 118 measurements (grid separation 0.222 in.) made on a 3 in. diameter phosphorus-diffused p-type silicon wafer. The mean sheet resistance $\overline{\rho_s}$ is indicated at the lower left and the uniformity, defined* as $\pm 2\sigma\sqrt{\rho_s} \times 100\%$ (σ is the standard deviation) is at the lower right of the map. As the interested reader may verify, when equal nu-

*This definition of uniformity accounts for 95% of all readings if the data are distributed normally.

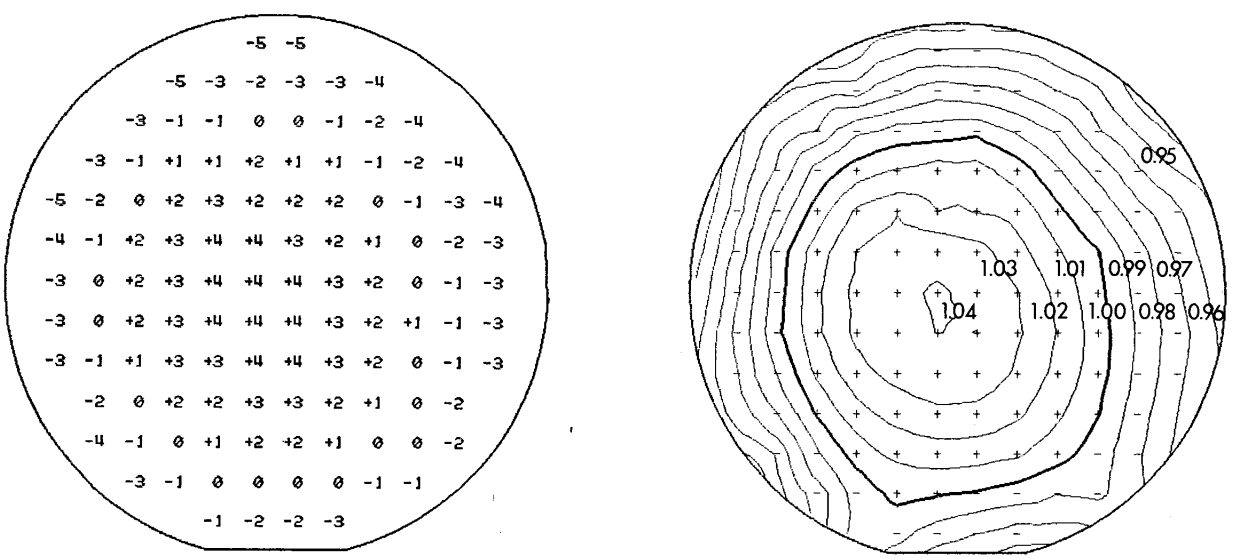


Fig. 1—(a) Deviation map and (b) contour map for a phosphine diffusion (middle of boat).

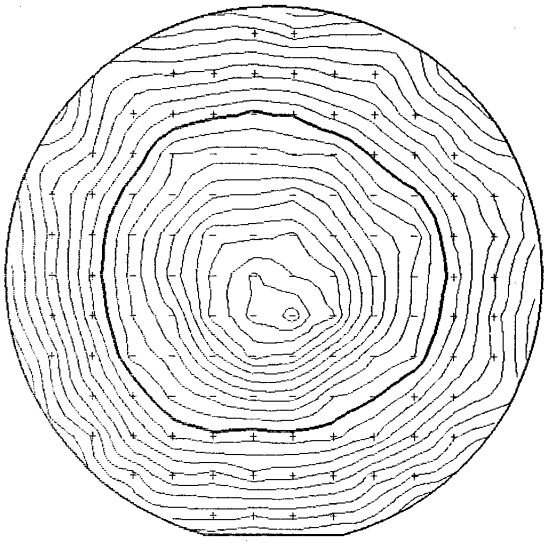


Fig. 2. N-type substrate (7 ohm-cm).

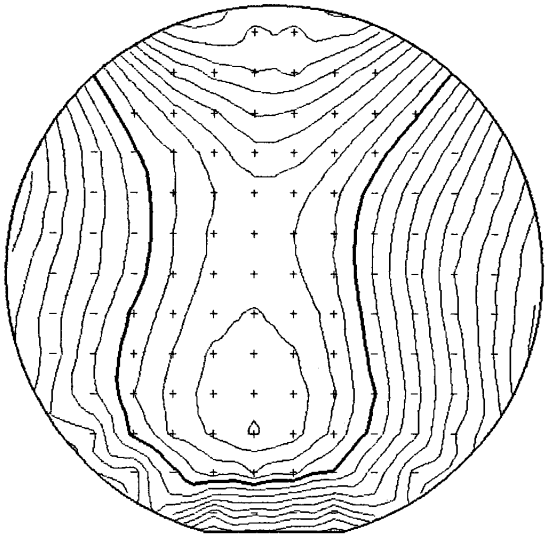


Fig. 3—N-type epitaxial layer (1 ohm-cm).

merical values are grouped in Fig. 1a by sketching a series of closed contours, a radial pattern of variation emerges. Figure 1b illustrates this method of treating the data using iso-sheet resistance contours constructed by a specially developed computer program operating in conjunction with a high-speed electrostatic plotter. The heavy contour line (labeled 1.00) represents $\overline{\rho_s}$, while the lighter contour lines (labeled . . . 0.98, 0.99, 1.01, 1.02 . . .) differ from $\overline{\rho_s}$ in increments of 1%. The symbols +(−) signify the location of experimental points whose resistance values are greater (less) than $\overline{\rho_s}$. Values of ρ_s which fall outside of pre-assigned sorting limits are represented by the symbol *.

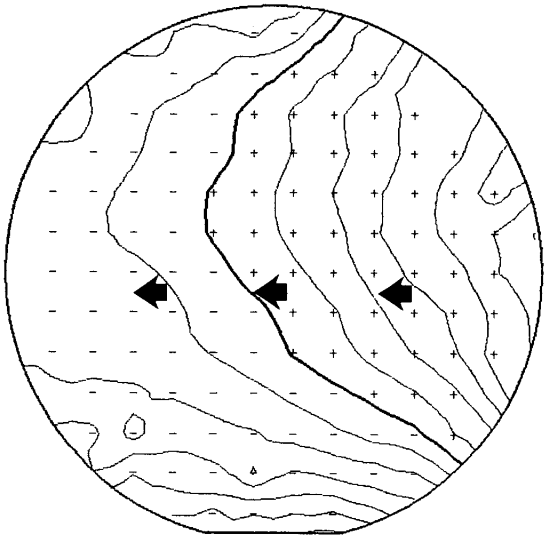
The authors have found "1%"-contour maps to be a dependable and effective means of disclosing the spatial distribution of impurities and the variations in film thickness which are characteristic of semiconductor processes. In the following sections, a brief process "inventory" is presented which serves to reveal the non-uniformity in some typical processes. In each case, the data have been obtained from 3 in. diameter silicon wafers.

Non-Uniformity in Sheet Resistance

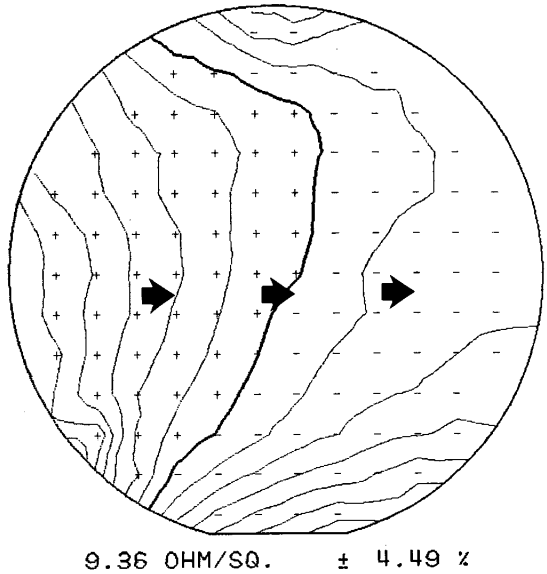
Sheet resistance is the parameter most widely used to monitor impurity content because of the convenience with which it can be measured both in and out of the wafer fabrication area. Various test vehicles are used for this purpose including the four-point probe, resistor geometries, and van der Pauw patterns.[6]

The data to be presented in this section were obtained using standard in-line four-point probes either in conjunction with photolithography defined rectangular test patterns or on otherwise unprocessed wafers.[4] This approach facilitates the characterization of doped wafers by minimizing the number of operations which must be performed prior to testing.

The test system employed for the acquisition of sheet



(a)



(b)

Fig. 4—Phosphine diffusion with flow from (a) right to left and (b) left to right (wafers faced each other in the source end of a diffusion boat).

resistance data consisted of an x-y wafer prober, prober control, data terminal, recording devices, and sequencing and interface modules. A minicomputer with associated program and system disk drives, tape reader and terminal were employed for analysis. Display of the data in the form of contour maps was achieved using a high speed electrostatic printer-plotter.

A. *Starting Material*

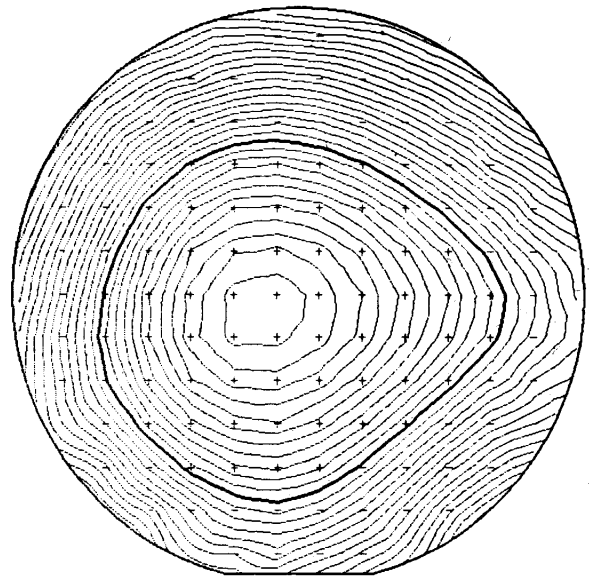
Figure 2 represents an n-type <111> orientation Czochralski-grown silicon wafer. The doping gradient (highest concentration at the center of the wafer) is a consequence of the segregation of phosphorus during the growth of the silicon ingot. The value $\rho_s = 201.7$ ohm/sq. corresponds to a resistivity of 7.0 ohm-cm.

Figure 3 illustrates the variation of resistivity over an n-type layer epitaxially grown on a 15 ohm-cm p-type silicon wafer. The tear-drop pattern reflects the spatial distribution of the reactant gases during the growth cycle. The value $\rho_s = 1026.9$ ohm/sq. corresponds to a resistivity of 1.0 ohm-cm.

B. *Gaseous Diffusion Source*

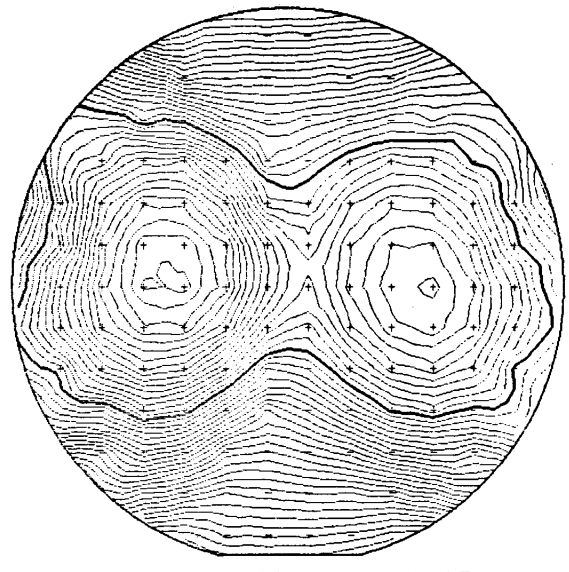
Figure 4 shows two contour maps for wafers placed face-to-face in the "source"-end of a standard quartz ladder boat. A flow of phosphine gas was maintained parallel to the face of each wafer, as indicated by the arrows. The maps exhibit patterns which are attributed to the dopant gas cooling the leading edge of each wafer. The fact that the contour maps of Figs. 4a and 4b are mirror images, and that the corresponding statistical parameters ρ_s and σ agree to better than 1%, is consistent with the face-to-face positioning of the wafers within the diffusion boat.

Figure 5 is a contour map for a wafer placed in the middle of a fully-loaded, slotted quartz diffusion boat. In this case, a flow of arsine gas was maintained parallel to the face of the wafer. The resulting distribution of im-



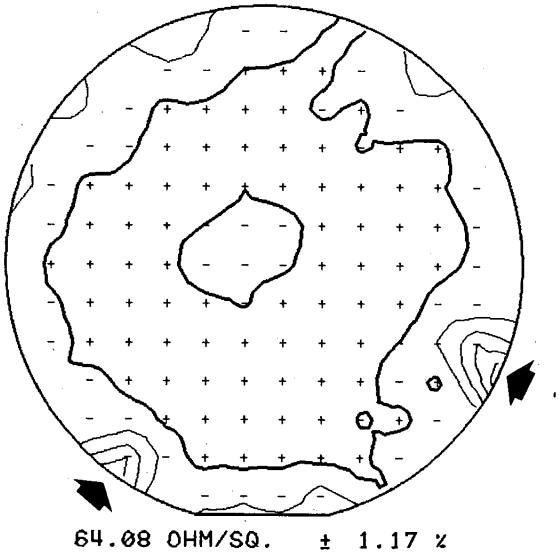
23.20 OHM/SQ. ± 13.25 %

Fig. 5—Arsine diffusion (wafer fully shielded).



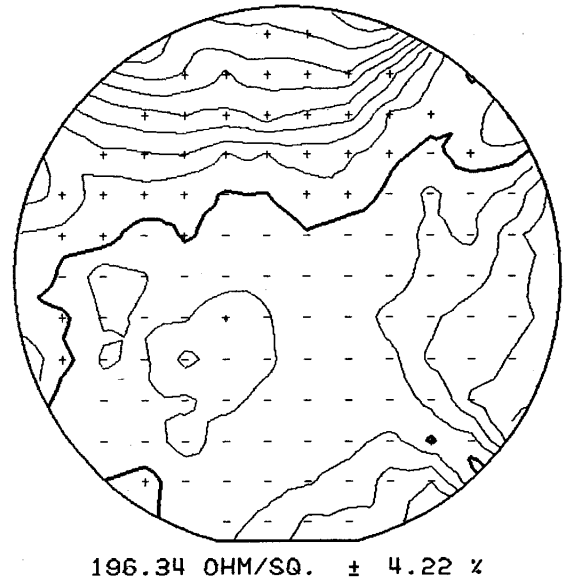
19.09 OHM/SQ. ± 19.35 %

Fig. 6—Arsine diffusion (wafer partially shielded).



64.08 OHM/SQ. ± 1.17 %

(a)



196.34 OHM/SQ. ± 4.22 %

(b)

Fig. 7—(a) Boron nitride deposition and (b) same wafer after diffusion.

purities is radial; the doping is a minimum (ρ_s maximum) at the center of the wafer. Figure 6 is a contour map for a wafer diffused under the same conditions as those for the wafer of Fig. 5. This wafer, however, was partially shielded by two other wafers occupying an adjacent slot of the diffusion boat, evidence of which is given by the resistance maxima located at the left and right sides of the wafer. The top and bottom of the wafer, which were not shielded, are doped to a significantly greater extent than the rest of the wafer.

C. *Planar Diffusion Source*

Figure 7a represents the variation in sheet resistance obtained by using a boron nitride planar diffusion source. The features identified by the bold arrows correspond to the location of the quartz rods used to support the wafer during the diffusion operation. Figure 7b represents the same wafer after an 1150°C diffusion in a wet oxygen ambient. The excellent uniformity achieved during the boron nitride pre-deposition cycle (Fig. 7a) is no longer present in Fig. 7b. This behavior is not unexpected, since a large fraction of the impurity contained in the initial shallow layer has been taken up by the oxide grown in the subsequent diffusion step.

D. *Ampoule Diffusion*

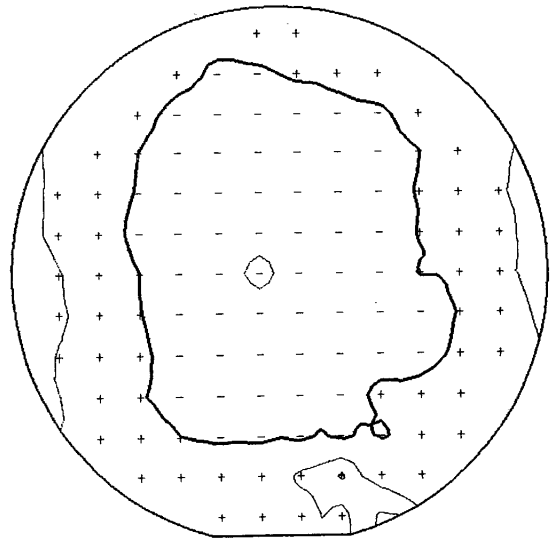
The contour map of Fig. 8 was obtained from a wafer subjected to arsenic diffusion inside a sealed quartz ampoule. The overall uniformity is significantly better than that achieved by using a gaseous source (cf. Figs. 5 and 6). The irregularity in the contour lines is associated with random measurement error originating in the mechanical tolerances of the four-point probe assembly.

E. *Ion Implantation*

Ion implantation offers a degree of doping uniformity which is generally superior to that of conventional diffusion technology. There are, however, geometric effects in electrostatic scanning and velocity effects in mechanical scanning implantation systems which limit the attainable uniformity.[4]

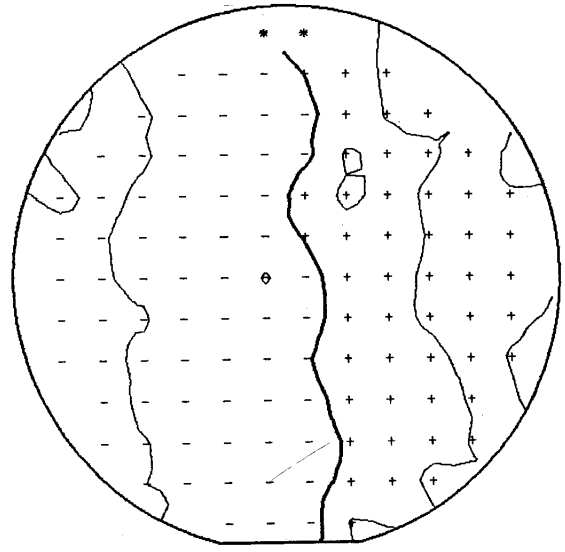
Figure 9 is an example of a wafer implanted in a system employing electrostatic scanning of the ion beam. The wafer was rotated with respect to the incident beam through an angle of 7° about an axis passing through its left edge, perpendicular to the flat. The contour map exhibits a characteristic doping gradient which is associated with variations in the cross-sectional area intercepted by the incident ion beam as it traverses the wafer.[4]

Figure 10 is a representative contour map of a wafer implanted in a system employing mechanical scanning through a stationary ion beam. The band across the midsection of the wafer is more lightly doped than the upper and lower portions of the wafer. This behavior is a consequence of the central portion of the wafer moving more rapidly than its edges through the ion beam. (The velocity variations are associated with the design of the mechanical system used to move the wafers.) The overall 2σ-uniformity of $\pm$ 1.00% agrees well with the predicted value of $\pm$ 0.70%.[4]



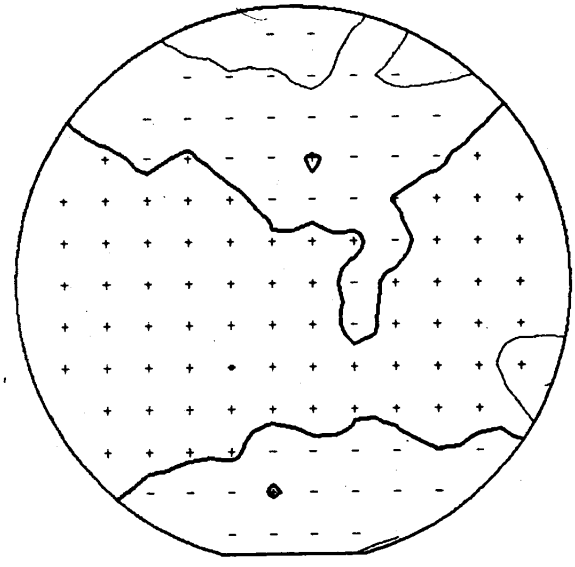
9.16 OHM/SQ. ± 1.07 %

Fig. 8—Arsenic capsule diffusion.



147.02 OHM/SQ. ± 1.83 %

Fig. 9—Ion-implantation (electrostatic scanning).



34.45 OHM/SQ. ± 1.00 %

Fig. 10—Ion-implantation (mechanical scanning).

C. *Deposited Phosphosilicate Glass*

Phosphosilicate glass is commonly used in semiconductor processing as passivation, for gettering mobile impurities, as a scratch-protection layer, and in applications requiring a fast-etching layer. The contour map of Fig. 14 represents the variations in thickness for a layer of phosphosilicate glass deposited at 400°C. In the four-wafer system employed, reactant gases (phosphine, silane, oxygen) are mixed and dispersed through separate nozzles in close proximity to each wafer. The pattern of variation shown in Fig. 14 is associated with a non-uniform temperature distribution characteristic of the hot-plate employed in this type of deposition system.

D. *Silicon Nitride*

Silicon nitride is receiving increasing use as a dielectric in semiconductor processing. Its ability to act as an etch-mask and oxidation barrier for silicon dioxide makes it possible, for example, to fabricate oxide-isolated bipolar transistors for circuit applications requiring a high density of active devices. The contour map of Fig. 15 represents the variation in thickness for a film deposited at 920°C in an r.f.-heated horizontal epitaxial reactor used exclusively for the deposition of silicon nitride. The contour map exhibits a pattern which is associated with the flow of reactant gases (silane, ammonia, hydrogen) along the length of the susceptor.

Application of Wafer Maps

The examples discussed in the preceding sections exhibit distinctive patterns which are generally a consequence either of inherent limitations in processing equipment or of the manner in which such equipment is employed when handling a large number of wafers. For example, while diffusion tubes are capable of providing long flat (± 0.5°C) temperature zones, the actual temperature distribution over wafers in a fully loaded fused silica boat will depend on such factors as mass and design of the boat, orientation of the wafers (parallel or perpendicular to the axis of the tube), and the wafer spacing. This behavior is illustrated by Figs. 1b and 4, which show the consequences of temperature variations over wafers situated, respectively, in the middle and source ends of a diffusion boat.

Wafer maps provide one with the ability to assess the influence of various operational parameters on wafer uniformity. Once these parameters have been established, periodic testing may be sufficient to verify that control is being maintained. Figure 16 illustrates the use of wafer mapping for controlling the performance of an electrostatically scanning implantation system operating in a production fabrication area. The target sheet resistance is 150 ohm/sq for a 5 x 10^{14} cm^{-2} 155 keV boron implanted layer. The broken lines for ρ_s = 135 and 165 ohm/sq represent ± 10% limits within which it is desired to maintain all sources of process variation. The mean sheet resistance and $\pm 2\sigma$ range of variation is indicated by the closed symbol and the vertical line centered upon it. Since the contour maps can be made available within hours of the wafer being implanted, erratic behavior can be detected and the cause investigated before implanting large quantities of wafers. The contour

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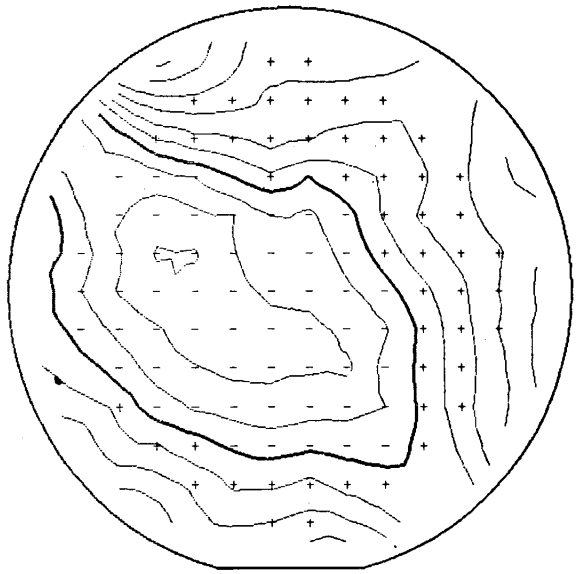

Fig. 14—Deposited phosphosilicate glass.

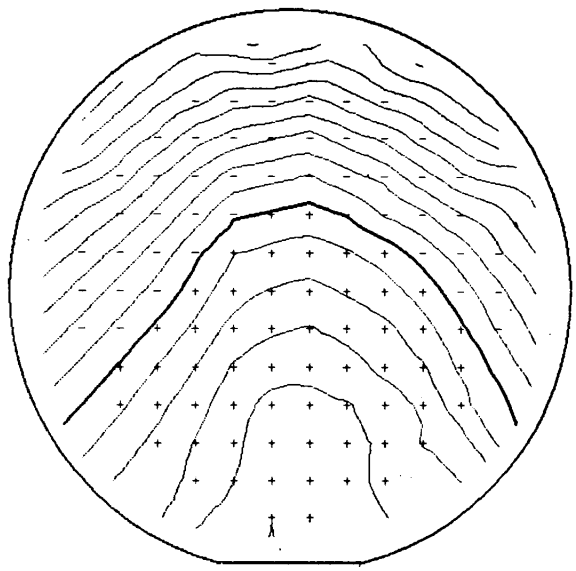

Fig. 15—Silicon nitride film.

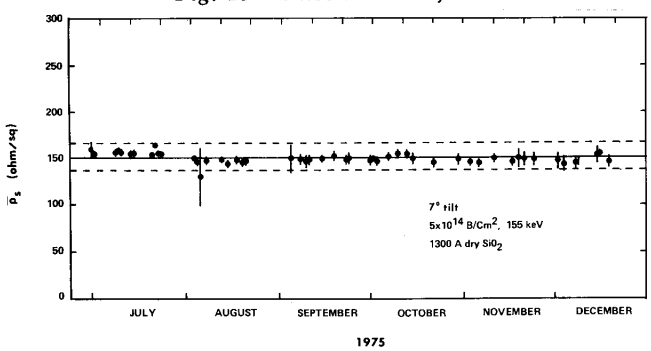

Fig. 16—Process control data for an electrostatically scanning implantation system.

Contour Maps

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map itself may help to identify the source of variability by exhibiting a characteristic pattern such as that associated with residual gas neutralization, in which the central portion of the wafer receives excessive doping.[4]

Conclusion

Distinctive patterns of non-uniformity exist in semiconductor processes which may be disclosed through the use of contour maps. A brief process "inventory" has been presented which includes examples indicative of the spatial variations which occur in doping, composition, and film thickness. These techniques, which have been applied by the authors in various diagnostic, development, and control applications, have led to a substantial improvement in the understanding and utilization of semiconductor processes. In the future, contour mapping is expected to play an important role in developing systems in which generic sources of variability—particularly those associated with processing wafers of diameter greater than or equal to 4 in.—are minimized.

Acknowledgement

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